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Thyristor Switched Capacitor Mitigation System for Customer Side Applications

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THYRISTOR SWITCHED CAPACITOR MITIGATION SYSTEM FOR CUSTOMER SIDE APPLICATIONS

By

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Thyristor switched capacitors (TSCs) have found an ever increasing role in the operation of flexible AC transmission systems or FACTS. The ability of these static var compensators to regulate the voltage by consuming or supplying reactive power quickly is not only viable for transmission but is an effective measure for increasing power quality at a distribution level. The proposed design uses a variable number of logically switched capacitors to supply reactive generation per reactive demand. The design ensures that the capacitors are safely switched into service, reactive demand is accurately calculated, and the TSC will respond quickly to changes in demand. While providing fast and safe operation, the conceptual design is also flexible enough to allow for optimization of the TSC to meet the demands of specific loads.

DEDICATION

I would like to dedicate this research to my parents Charles and Virginia Taylor and to my brother Jeremy. Without their humor and support I would never have believed I could make it this far.

ACKNOWLEDGEMENTS

I thank everyone that has aided me in completing this research and thesis. I especially extend my gratitude to my major professor Dr. S. Mark Halpin. Without his expert insight and support, this work could not have been possible. I thank my other committee members, Dr. Noel Schulz and Dr. Stanislaw Grzybowski for their patience and guidance.

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CHAPTER I

INTRODUCTION

The use of static var compensators (SVCs) has significantly increased in the transmission and distribution of electrical power during the past decade. These devices provide flexible control of reactive power flow and have allowed for increased power transfer capabilities at a lower cost than traditional system improvements. Besides being a cheaper solution, in most situations an SVC can be purchased and installed in less time than it takes to implement other methods that provide equal amounts of voltage stability [1]. The relatively low cost and flexibility of SVCs' have contributed to their use at commercial and industrial locations where the reactive power consumption is high and the delivery system is weak in its ability to provide rated voltage.

Because not all customers on a defined system may demand such high levels of reactive power, application of a mitigation device at the utility level may not be cost effective or necessary. Because corrective devices located on the utility side are required to handle all system conditions and loading demands placed on the entire system, any major change in the system may require a redesign of the SVC, while devices located on the customer side can be designed specifically for the load independently of the power system. In addition, locating the SVC at an industrial location permits the system improvement cost to be minimized further due to relatively smaller ratings than would be

required on the utility side [1]. Locating the SVC at the customer locations then provides not only a device specifically designed for the reactive demand but also a cost-effective solution.

The purpose of this thesis is to propose a design of a thyristor switched capacitor, a type of SVC, for operation in industrial environments. This design will respond quickly and accurately to counteract the problem of large reactive power variations found in industrial environments.

Background

Static var compensators are often used in electrical systems to sense and control the reactive demand of loads. The first static var compensator was demonstrated and commercialized by General Electric in 1974 and Westinghouse followed with a model in 1975 [2]. Both were designed for use in transmission level operations. Today the use of SVCs is not only in transmission but in distribution and customer side electric systems as well. Static var compensators are composed of shunt connected static reactive power generators and/or absorbers whose outputs are varied to control the flow of reactive power to meet specific system operating conditions. The term static is used to reference that the device has no rotating or moving components.

A subset of SVCs is the thyristor switched capacitor (TSC). Thyristor switched capacitors typically consist of two to five shunt connected capacitor banks that are individually switched fully on or off. Each bank of a TSC is connected in series with a bi-directional switch consisting of back-to-back connected thyristors. The use of a bi-directional switch allows the TSC to be controlled every half cycle. The thyristor is the

most prevalently used switching device due to its ability to withstand high current. This has led to use of its name in the device. Even though it is not always necessary to use thyristor semiconductors in every TSC design, this naming convention will be used throughout the document to keep it standard with other forms of literature on the subject. An example diagram of a standard TSC configuration is shown in Figure 1.1.

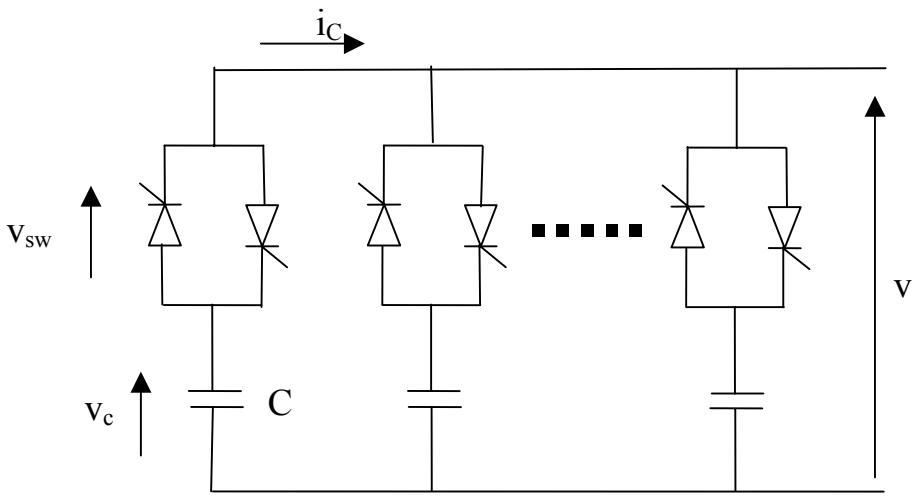

Figure 1.1: Example Diagram of TSC

In order to eliminate transients, the switching point of TSCs are controlled such that they occur when the voltage across the capacitor is equal to the applied voltage. Gating the thyristors at a non-zero value would result in a large transient current as shown in Equation 1.1.

$$i_c = C\frac{dv_c}{dt} \tag{1.1}$$

When the thyristor switches are gated, the steady-state current through any branch can be defined relative to the input voltage as shown in Equations 1.2 and 1.3. When performing system studies, the voltage drop across the thyristors is assumed to be zero because of its relatively small value when compared to the system voltages. However, the voltage drop across the thyristor will play a significant role in the thermal considerations when sizing the solid-state device.

$$v(t) = V\sin(\omega t) \tag{1.2}$$

$$i(t) = V\omega C \sin(\omega t + \pi/2) \tag{1.3}$$

When the gate pulses are removed, the thyristors continue to conduct current until the current passes through the zero point. Because the current through the capacitor leads the voltage by 90°, the potential held by the capacitor correlates with the peak amplitude of the voltage. Due to this charge, the voltage across the non-conducting thyristors will be the applied ac voltage minus the dc offset of the charged capacitor. The polarity of the dc offset will depend on the specific half of the cycle in which the gate signals were removed. When the switching circuit is gated again, it is vital that the gating signal occurs when $v - v_c = 0$. This is necessary because this point corresponds with the zero crossing of the current and the point when the instantaneous voltage is equal to the charged capacitor voltage. If this condition is not met then a large transient current will occur causing potential damage to the equipment. Therefore, the capacitor banks may be switched off every half cycle of the applied ac voltage, but they may only be switched on once per cycle. This operation requirement has lead to the use of thyristor/diode pairs, which in effect will limit the turn off capabilities to once per cycle. Thyristor/diode pairs

are cheaper than two separate thyristors and provide switching control without sacrificing performance of the unit. Figures 1.2 and 1.3 show the graphs of the voltages and currents across one branch of a TSC during switching operations assuming back-to-back thyristors are used.

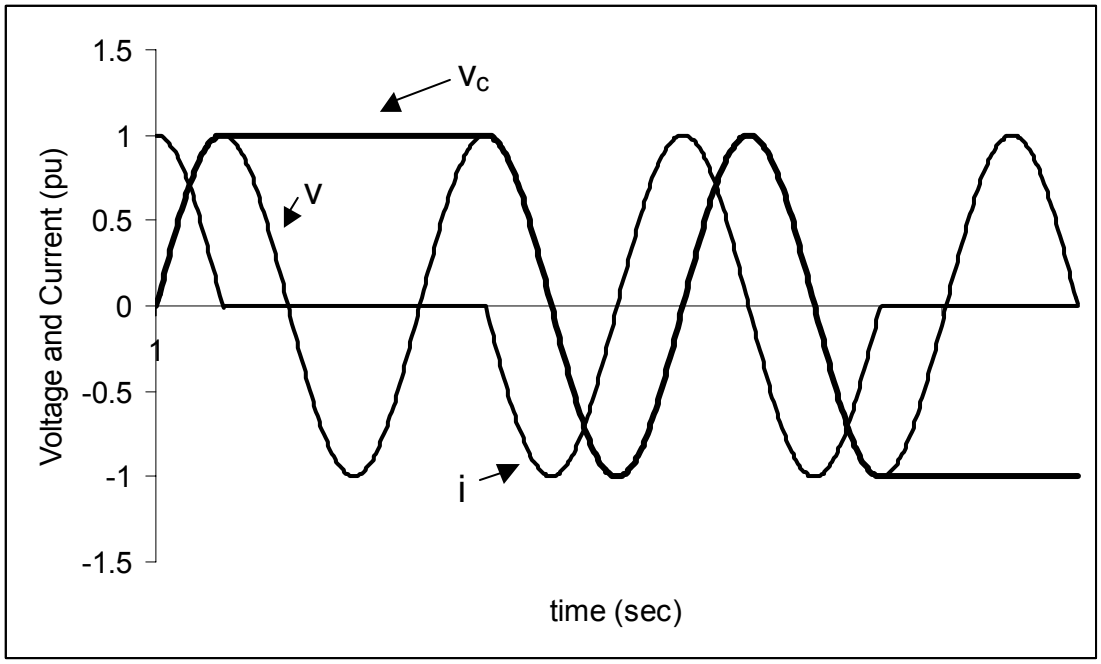

Figure 1.2: Switching Operation of TSC

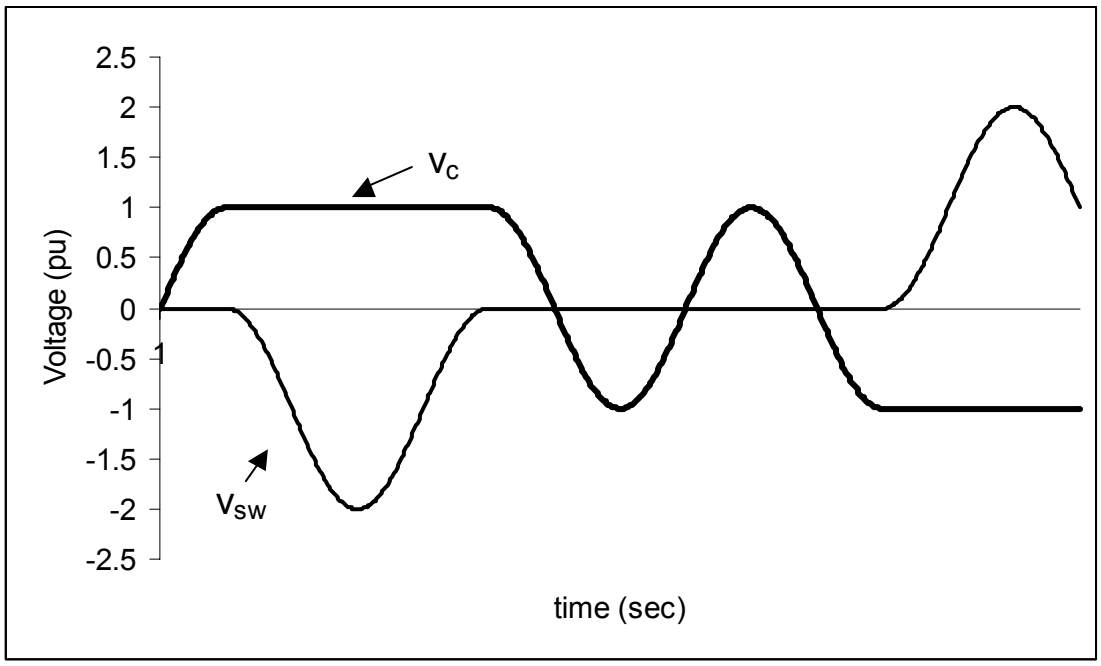

Figure 1.3: Switching Operation of TSC

The capacitor banks of a TSC are switched on as needed in response to reactive demand. As the reactive demand changes, a control system calculates the reactive power consumption and switches in the appropriate number of capacitors to limit the amount of reactive power flowing through the system. Each switched capacitor bank results in a step in the reactive power supplied, and therefore the reactive generation produced by a TSC takes the form of a stepwise response to a linear increase in reactive demand. As shown in Figure 1.4, the stepwise response of a TSC is limited by the amount of capacitance available. This stresses the importance of sizing the TSC to handle the loading conditions it is implemented to counteract.

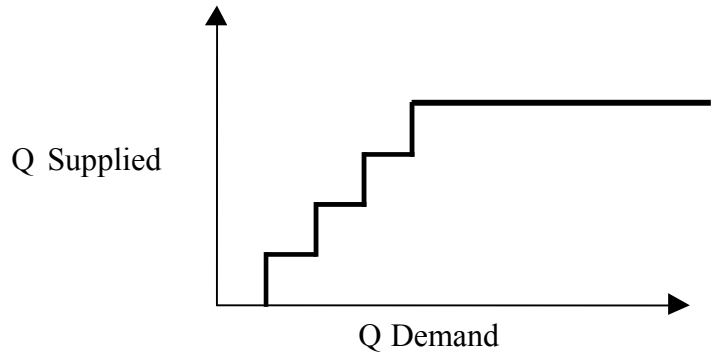

Figure 1.4: Stepwise Output of TSC

Load Characterization

Thyristor switched capacitors regulate voltage by quickly supplying reactive power, which acts with the system impedance to raise voltage levels. It is crucial that a working knowledge of the system characteristics and the loads applied to the system are obtained before a TSC can be designed and implemented correctly. Locating a TSC at an industrial site requires designing the device to counteract the reactive demands of arcing loads, large induction motors, and other widely varying reactive loads. In addition, utilities normally place restrictions on the voltage variations due to customer loads. It is therefore important to define the extent and frequency of the fluctuations in reactive power demand and their effects on the electrical system.

One of the best methods for determining load characteristics is on site data collection. Capture of small time scale operations of the loads will be vitally important because the reactive demand can fluctuate quickly. It will also be necessary to record

data during extended periods to determine the operating procedures of the load and their effects on the system. An example would be a large electric arc furnace operated during different periods of the day. Electric arc furnaces are non-linear time varying loads. This makes them difficult to model and gathering on-site data is essential to determine their effect on the system. If measurements of the furnace are taken only during times when the system is lightly loaded the effect the increased reactive demand has on system voltage levels will not be captured. Evaluating the minimum reactive power consumption that generates undesirable voltage fluctuations is also significant. If the capacitors of a TSC are sized too large, the mitigating device will either be unable to respond to the changes in reactive demand or it will respond with too large of a step in supplied reactive power. Therefore accurate on site data collection is essential when characterizing the loads and consequently when designing the applied TSC.

There are situations where on-site data collection is not possible or practical. In these cases, data collected from similar loads can be used, or computer modeling of the equipment and power system can be used to predict variations in reactive power. A situation where modeling of the load and system can be helpful is during the evaluation of large plants at the end of weak distribution feeders. The use of large induction motors for pumping stations is a prime example. The parameters for motors used in pumping stations are typically known, or can be reasonably estimated, and therefore can be modeled with the system in order to calculate the severity of voltage drop during motor start. Equation 1.4 provides a method for estimating voltage drop at the motor based on power system and motor apparent power characteristics.

$$V_{min} = \frac{V \bullet kVA_{SC}}{kVA_{LR} + kVA_{SC}} \tag{1.4}$$

where

V = actual system voltage in per unit of nominal

kVA_{SC} = system short circuit apparent power at the motor

kVA_{LR} = motor locked rotor apparent power

While the method in Equation 1.4 uses apparent power in the calculation of the voltage drop, the majority of the power drawn in by the motor during start up is reactive. Figure 1.5 shows the power demand for a modeled induction motor. When the motor is started a large amount of reactive power is drawn by the motor. In fact, large induction motors are able to draw several times their full load power consumption during starting with a power factor usually in the range of 30 to 50% lagging [3]. While there are many methods to limit the voltage drop caused by motor start up, these may or may not be applicable due to the complexity of implementation for a large number of motors, the reduced torque during start up, or not being able to compensate for widely varying reactive demands after start up. TSCs have the capability to correct this voltage drop issue while addressing the previously stated problems.

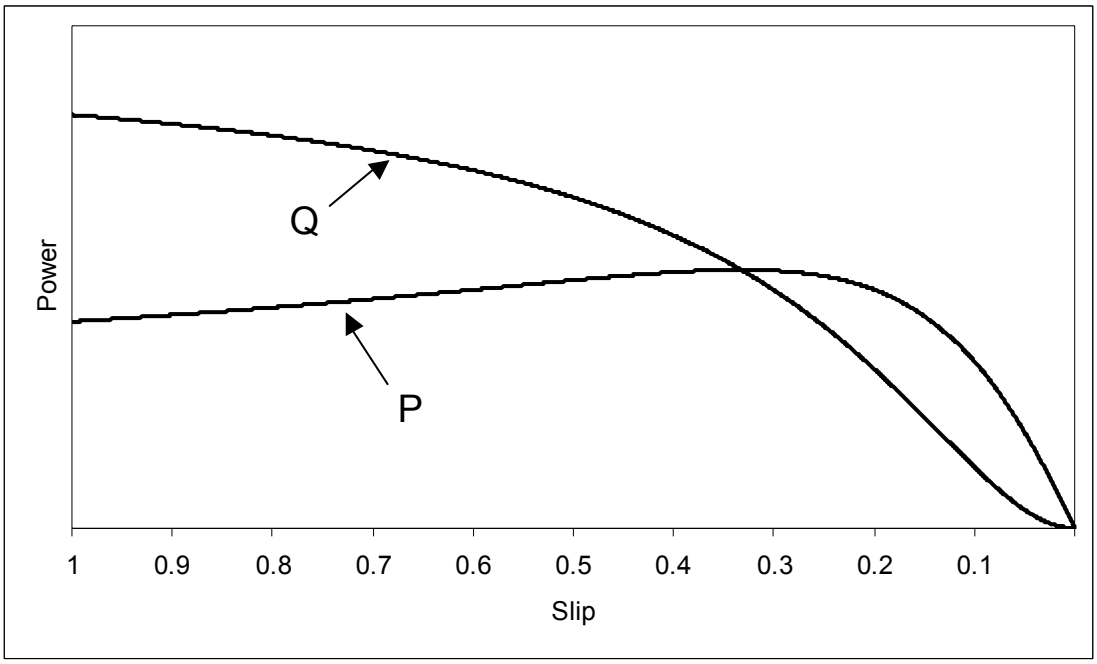

Figure 1.5: Real and Reactive Power Demand vs. Slip

CHAPTER II

DESIGN REQUIREMENTS

The proposed design of the thyristor switched capacitor warrants a number of requirements for the mitigation device:

1. Applicable to customer side voltages and power requirements;
2. Minimal overall cost and complexity of the installation;
3. Natural convention heatsink cooling for the solid-state devices;
4. Modular design of components;
5. Cycle to cycle control of the thyristor switched capacitor gating; and
6. Large total reactive generation capability provided in small steps.

The first two requirements are met by designing the TSC to be located at the industrial or customer location. The other requirements are fulfilled by the individual components of the TSC.

Figure 2-1 shows the proposed thyristor switched capacitor system for an individual phase. It consists of three main general functional blocks: the PC-104 controller is used to calculate the reactive power and implement the gating decision algorithm, the gating circuit controls the switching such that transients are eliminated, and the TSC banks consisting of semiconductor switches and capacitors. Note that each capacitor bank has a solid-state switching device and a corresponding gate control circuit.

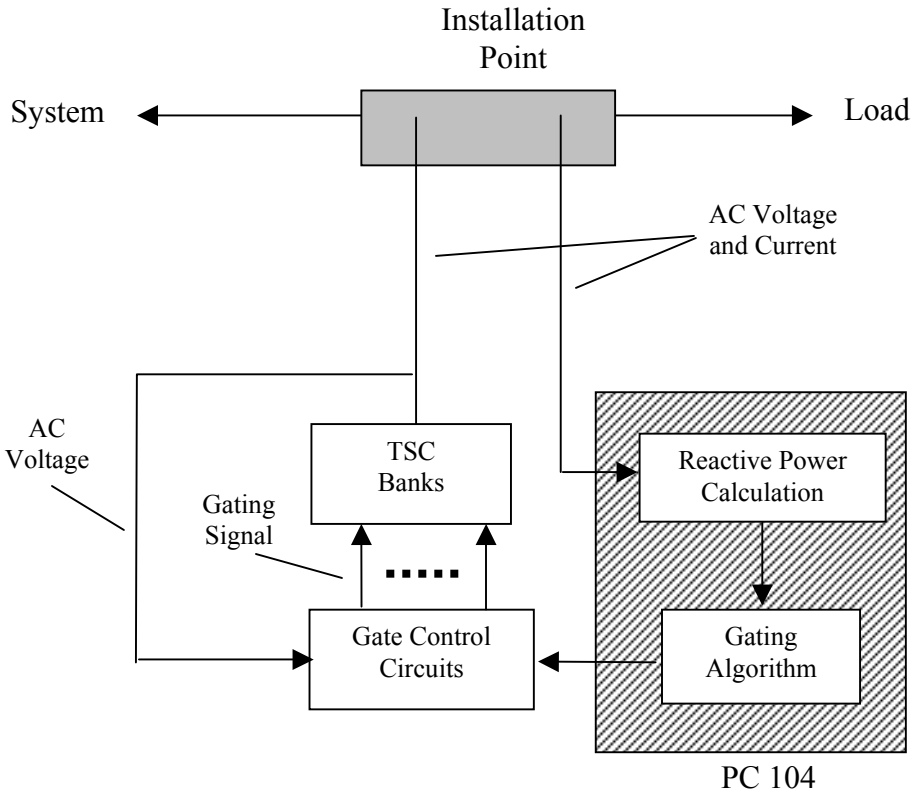

Figure 2.1: Thyristor Switched Capacitor Configuration

To insure a small step size with a large amount of potential reactive generation, the capacitors were selected in sizes of common binary multiples. This configuration would allow for 2^n steps per phase and would minimize the number of capacitors required. To illustrate, selecting four capacitor banks of sizes of 10, 20, 40, and 80 kvar would allow for a maximum reactive generation of 150 kvar per phase and a step size of 10 kvar. By selecting this configuration of capacitors, it is possible to meet the reactive generation requirements to within ±5 kvar up to 150 kvar. The max error is half of the smallest rated capacitor unit, and therefore the proposed system will be accurate to within ±½ the smallest kvar size.

CHAPTER III

SWITCHING APPARATUS

While thyristor devices are prominent in the design of static var compensators, they are not always a necessity for every design. In this case, Insulated Gate Bipolar Transistors or IGBTs were considered because of their gating simplicity and their ability to handle medium power levels. At the present, IGBTs are available with ratings as high as 1700 V and 1200 A, with substantially higher ratings projected for the future [4]. Another advantage of IGBTs is that they are produced in modules containing a free wheeling diode connected anti-parallel to the IGBT. These modules will simplify the control scheme, while still providing adequate ratings for voltage and current.

While the IGBT modules offer sizable ratings, the cooling for the IGBT is limited. By limiting the cooling measures to only natural convection heatsinks, the maximum power the IGBT can switch is reduced further than the given ratings. Consequently, the ability of the IGBT and its heatsink to dissipate heat will define the maximum capacitor size.

The method for establishing an estimate of the thermal capabilities of an IGBT module, such as shown in Figure 3.1, is established by the manufacturer and is given in Equation 3.1 to 3.3 [5]. The equations provided are based on the assumption that the solid-state device is being switched only at the safe switching points. Thus the hard

switching losses are neglected and losses across the IGBT module will be composed of purely conduction losses. The limit on the capacitor sizing is then directly related to the ability of the IGBT and heatsink to conduct excess heat resulting from the conduction losses.

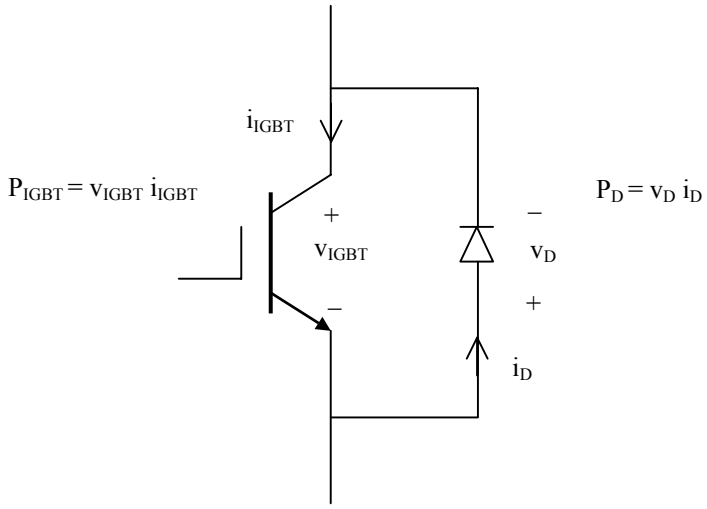

Figure 3.1: IGBT with Free Wheeling Diode

$$T_C = T_A + (P_{(IGBT)} + P_{(D)}) * (R_{SA} + R_{CS}) \tag{3.1}$$

$$T_{J(IGBT)} = T_C + P_{(IGBT)} * R_{JC(IGBT)} \tag{3.2}$$

$$T_{J(D)} = T_C + P_D * R_{JC(D)} \tag{3.3}$$

where the known values given by the device manufacturer are:

R_{SA} = sink to ambient thermal resistance

R_{CS} = case to sink thermal resistance

R_{JC} = junction to case thermal resistance of diode or IGBT

and the values to be evaluated are:

T_A = ambient temperature

T_C = case temperature

T_J = junction temperature of diode or IGBT

P_{IGBT} = power dissipation of the IGBT

P_D = power dissipation of the diode

Because the cooling for the solid-state devices is limited by the requirement to use convection only cooling, the issue is not finding sufficient cooling for a given power rating. Rather the issue is what power level the device can safely and reliably switch. Therefore the best possible combination of heatsink and IGBT was selected and evaluated for its ability to dissipate heat for various levels of loading and fixed ambient temperature. In other words, evaluations of the junction and case temperatures were made for set values of the thermal resistances, ambient temperatures, and varying levels of conduction power losses. Numerous modules were evaluated for their capabilities under the limited cooling conditions and Powerex's CM600HU-12F provided the highest capability of 40 kvars.

Figure 3.2 shows an equivalent circuit based on Equations 3.1 to 3.3 using the data for the CM600HU-12F module with the conduction power losses represented as current injected into the circuit, the temperatures represented as the voltage values at the nodes, and the thermal resistances represented by electrical resistances. The CM600HU-12F data sheet is attached in the appendix and provides the maximum values for the case

and junction temperatures, as well as the internal thermal resistances of the module. The remaining thermal resistance is defined by the heatsink, and the ambient temperature is a design parameter based on the worse case temperature. In this case, the capacitors selected could withstand no more than 60° C and therefore set the maximum ambient temperature to which the unit could be subjected. While it is unlikely that the TSC will be placed in such harsh environmental conditions, the high value for ambient temperature will provide increased reliability in the design. This increased reliability will result in fewer component failures due to overload.

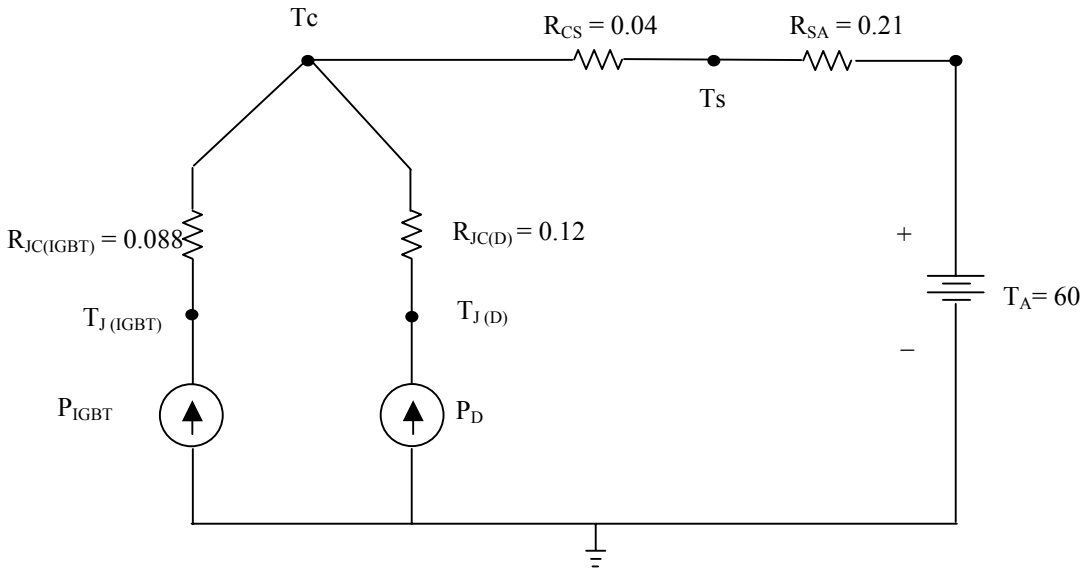

Figure 3.2: Equivalent Circuit of IGBT Module Heat Dissipation

Because of the diode and IGBT components having different magnitudes of saturation voltage, the power dissipation of both components must be evaluated independently, and therefore the voltage drop and rms current for both components must be calculated individually. Because the IGBT will conduct only during the positive half and the diode only during the negative half of the current waveform, the voltage drops across the diode and IGBT are composed of square waves. These square waves have magnitudes ranging from zero up to the saturation voltage. Thus, the effective or rms value of the saturation voltage for both diode and IGBT is calculated by the dividing the saturation voltage by 2. The rms current for the module, as a whole, is calculated directly by capacitor rating and the applied voltage. Again, the diode and the IGBT see only a half a cycle of current per period, therefore the individual rms currents are found by dividing the total rms current by a factor of $\sqrt{2}$. With the diode and IGBT rms voltages and currents known, the power dissipation across the IGBT and diode can be calculated. Calculation for the IGBT power dissipation using the CM600HU-12F is provided in Equations 3.4 to 3.6 for a 40 kvar 277 V_{LN} application. Similar calculations are required for the diode.

$$V_{RMS(IGBT)} = \sqrt{\frac{1}{1/60}\left[\int_{0}^{1/120}(2.2)^2 + \int_{1/120}^{11/60}0\right]} = \frac{2.2}{2} = 1.1 \quad V \tag{3.4}$$

$$I_{RMS(IGBT)} = \frac{Q_{RATED}}{V_{LN}\sqrt{2}} = \frac{40{,}000}{277\sqrt{2}} = 102.11 \quad A \tag{3.5}$$

$$P_{IGBT} = \frac{2.2}{2} * \frac{40{,}000}{277\sqrt{2}} = 112.2 \quad W \tag{3.6}$$

The values for the saturation voltages are obtained with the module operating at its maximum ratings and are therefore higher than their actual values during normal operation ranges. Again, the purpose of utilizing this worse case scenario in the calculations is to provide an extra measure of reliability when calculating the capabilities of the device.

With the ambient temperature modeled as a voltage source, the circuit of Fig. 3.1 can now be solved for the equivalent temperatures at each node. The tabulated results using the example device with the given conditions are given in Table 3-1. The maximum junction temperature, T_J, for the module is provided by the data sheet as 150° C, and the calculated results provides a solution less than the criteria. If the calculated junction temperature were higher than the criteria, the device would not be reliable under the given circumstances.

Table 3.1

Thermal Evaluation of Powerex's CM600HU-12F

TA	60	
Rsa	0.21	
Voltage	277	
R_{CS}	0.04	
$R_{JC(IGBT)}$	0.088	
$R_{JC(D)}$	0.12	
$V_{CE(IGBT)}$	2.2	
$V_{CE(D)}$	2.6	
	IGBT	**DIODE**
Vrms,drop	1.1	1.3
C (F)	1.383E-03	1.383E-03
kVAR	40	40
Irms	102.11	102.11
P (W)	112.3202	132.7421
Tc	121.2656	
Tj	131.1497	137.1946
MAX Tj	150	150

While paralleling of the IGBT modules does allow the ability to switch more capacitance, it will quickly add to the overall thermal requirements. With the common binary multiple configurations of the capacitors, the number of heatsinks required also grows in this manner after the 40-kvar limit is reached. For example, if capacitor sizes of 20, 40, 80, and 160-kvar rating were chosen eight heat sinks would be required.

Gate Drive Circuit

Control of an IGBT is slightly different from that of a thyristor. Where the thyristor is gated on by a current impulse and continues to stay on until the current passes through the zero point, IGBTs are gated on by applying a positive voltage to the gate for turn on and stops conducting when the voltage is removed. Therefore, transient free

switching of the capacitor requires that the gating signal be applied or removed only during the $v - v_c = 0$ points and held constant between these points. Figure 3.3 represents the proposed gating control circuit that will implement these requirements. The gating circuit is composed of three main functional blocks. These are the switching signal from the PC –104, the timing signal, and a latching device to hold the voltage constant during gating.

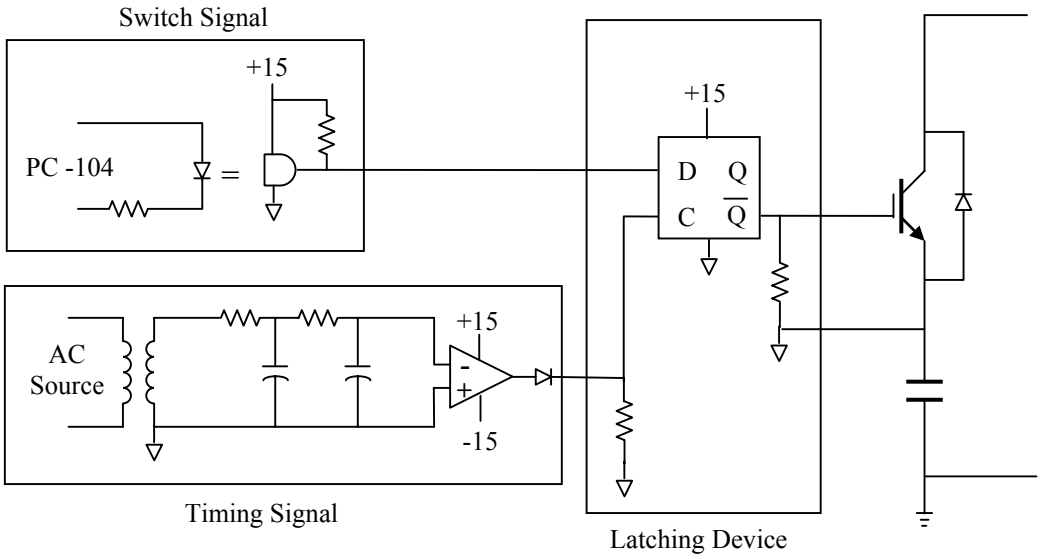

Figure 3.3: IGBT Gate Drive Circuit

Determining the proper switching points is the responsibility of the timing signal block, which creates a clock pulse based on the frequency and phase of the AC source for input into the latching device. Applying the AC signal to an overdriven inverting op-amp creates this clock pulse. Because the resistance between the negative and output terminals of the inverting op-amp is infinite, the output will be driven to the supply rails and is said to be overdriven or clipped. The resulting square wave has the same frequency as the AC

source, but because of the inverting configuration of the op-amp is 180° out of phase from the AC source. Because the capacitor must be switched during the points when the voltage source is equal to the negative peak voltage trapped on the capacitor, a 90° phase shift was introduced to the sinusoidal input in front of the op-amp. Using two RC low pass filters easily performed this phase shift. The square wave now has the desired phase shift of 90° leading the voltage source and the state changes correspond with the voltage zero crossings, but the signal must still meet the operating conditions of the latching device.

The latching device does not allow for negative voltages to be applied to its input, and therefore the clock signal must be altered to remove the negative half-cycle. Eliminating the negative half-cycle is performed simply by placing a diode at the output terminal of the op-amp. Connecting the lower rail of the op-amp to the reference in theory will provide the same square wave of zero to positive voltage pulses and eliminate the need for a negative voltage in the circuit. However, in practice this configuration did not provide a low voltage close enough to zero to prevent accidental switching or sufficient rise and fall times of the output signal. Using the diode to remove the negative half-cycle does fulfill the criteria required for correct operation of the latching device.

Besides having to remove the negative half of the clock signal, the state changes of the clock must correspond with correct state changes in the latching device to provide transient free operation. Because state changes for the selected latching device only occur during low to high changes in the clock signal, the low to high transition in the clock signal must correspond with transient free switching of the capacitors. Because the

IGBT is placed in the circuit such that it does not allow positive current to flow but the freewheeling diode allows the flow of negative current, the capacitor will charge to the negative voltage peak. Therefore the correct point for transient free operation occurs when the voltage source is at the negative peak. Because the clock signal already leads the voltage source by 90° the low to high transition for the clock signal already corresponds with this transient free switching point. The comparison between the final clock signal and the AC source is shown in Figure 3.4.

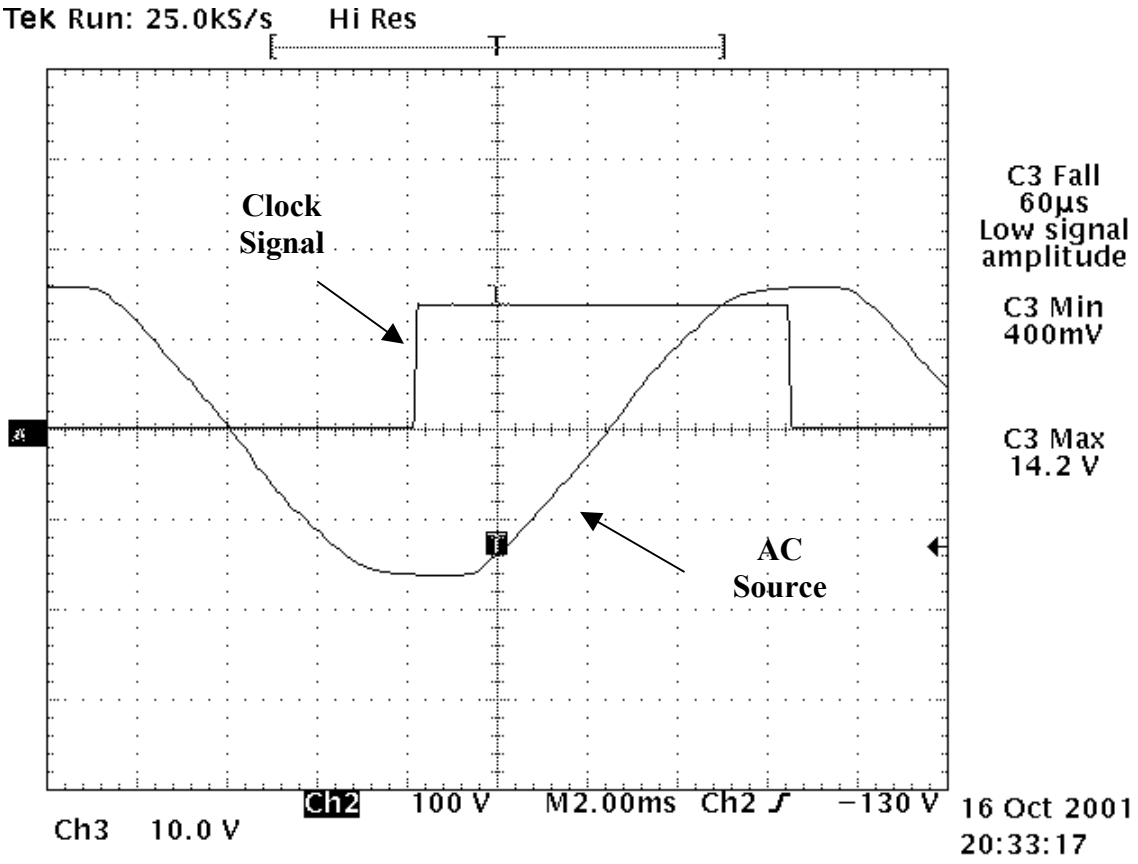

Figure 3.4: Clock Signal

The latching device is composed of a D flip-flop and resistors used to provide discharge paths to the reference. The D flip-flop latches the gating signal during a low to high transition in the clock and holds this signal until the next such change. Because the input to the D flip-flop had a significant amount of capacitance and the diode did not provide a path for the built up charge to dissipate to ground, the clock signal was distorted. Using a resistor connected to the input pin of the flip-flop and the reference allowed for the accumulated charge across the input capacitance to be discharged when the clock signal was low. The resistor connected between the gate of the IGBT and the

reference is also used in a similar manner to provide a path for capacitive charge across the IGBT from the gating signal, the gate to emitter voltage, to dissipate.

As specified in the data sheet for Powerex's CM600HU-12F IGBT module, a +15 V gate to emitter voltage, V_{GE}, is required for reliable gating of the IGBT. Because the emitter voltage is the same as the voltage across the capacitor, connecting the reference of the gating circuit to ground would not take into account changes in the emitter voltage. As a result, the reference of the gating circuit has to be tied to the capacitor such that it would float with changes in the capacitor voltage. By allowing for a floating reference, the flip-flop can supply the necessary +15 V to the gate relative to the emitter voltage.

The floating reference point resulted in the important design consideration of isolating the control equipment from the potentially high voltages of the floating reference. Protecting the control equipment was accomplished by using an optoisolator with a Schmitt trigger output to isolate the PC/104 DAC controller. The chosen optoisolator provided an isolation of 7500 volts for the controller, but operates with negative logic, and consequently the negated Q output from the flip-flop is used for the final gating signal to the IGBT. The isolation of the gating circuit gives it the ability to be applied to any type of IGBT independent of voltage level and the controller configuration or type.

The modular design of the gate drive circuit makes possible an extended number of other benefits. By providing a gate drive circuit per capacitor, any number of capacitor combinations can be configured quickly and easily. Failures within the drive circuit are contained within that particular unit and replacement does not require

removing the entire TSC from operation. The modular or black box configuration of the gating circuit also allows it to be used as a gate drive device for other types of solid-state devices. For thyristor switching, this is done by triggering a small IGBT connected in a pulse amplifier circuit configuration. Figure 3.5 gives the circuit's modification for thyristor switching.

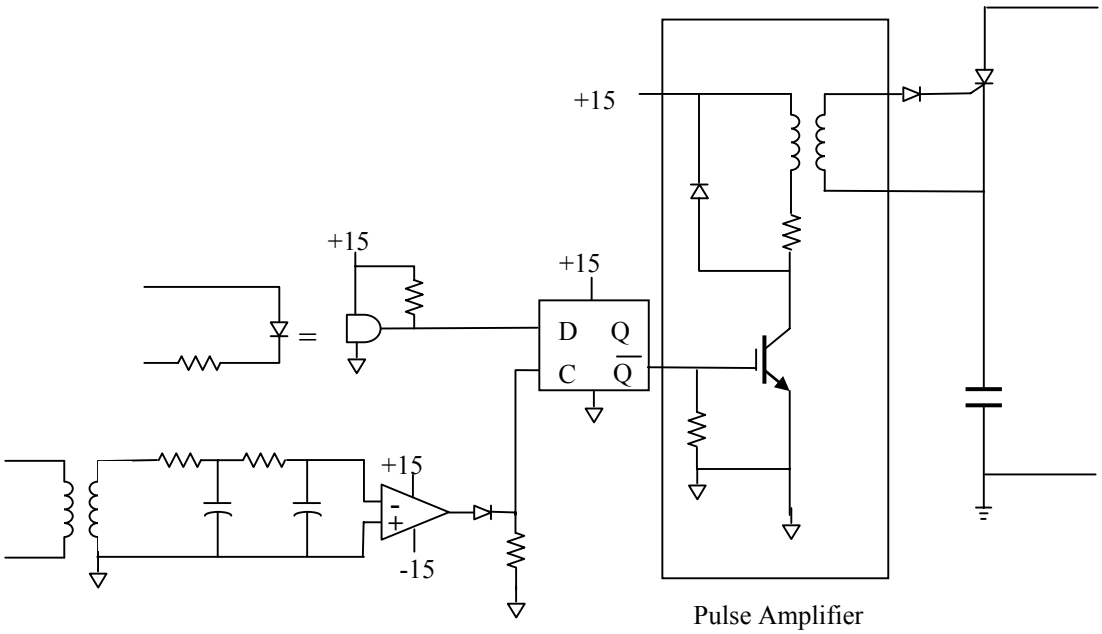

Figure 3.5: Gate Drive Circuit Modified for Thyristor Gating

When the IGBT is gated the change in current seen by the primary side of the transformer induces a current pulse on the secondary. This pulse can be amplified by the turns ratio of the transformer to gate the thyristor sufficiently. The diode on the

secondary side prevents the flow of negative gate currents and the primary side diode allows a path for the transformer magnetizing current to dissipate through the resistor.

CHAPTER IV

CONTROLLER

The benefits of the PC-104 architecture make it an optimum choice for the embedded controller. It is a PC based stackable module architecture that provides the ability to stack only the necessary components required for the embedded controller. This can appreciably reduce the size of the controller. If changes are later made in the functionality demands of the controller, additional modules can be added or removed as needed. The greatest benefit for this application is the PC-104 module's ability to handle excessive shock, vibration, and heat when compared to a standard PC. This is attributed to the secure stacking of the modules and using an entirely chip based design and a container resembling a large heat sink that not only protects the unit from damage but also dissipates any built up heat. PC/104 controllers are also more economical than traditional non-PC bus architectures such as STD, VME, and Multibus [6] and, as a PC based architecture, it is compatible with hardware and software of other PC based platforms.

The PC based architecture of the PC/104 permitted the creation of a software based control scheme fully implemented in code. This controller must be able to calculate quickly the reactive power demand and then decide how much of the available reactive generation needs to be switched in. Quick and accurate calculation of the reactive power

is key in effective operation of the TSC. Two methods are proposed here for the calculation of reactive power, the zero crossing method and the least squares method.

Zero Crossing Algorithm

The zero crossing algorithm is based on three consecutive operations; calculation of the rms voltages and currents, a phase lock loop filter, and the measurement of the reactive current at the zero voltage crossings. Due to properties of the phase lock loop, calculation of the rms voltages and currents must be determined first. Calculation of these values is performed using the discrete version of the true rms calculation, as given in Equation 4.1, where n is the number of samples in a ½ cycle. By performing the calculation with a half cycle worth of data, it is viable to calculate the rms value independently of where the samples begin during the cycle.

$$F_{RMS} = \sqrt{\left(\frac{1}{n}\right)\sum_{k=1}^{n} f^2(k))} \tag{4.1}$$

With the rms values of voltage and current known, the reactive power flow can be determined if the power factor angle is known as well. If the per unit values of voltage and current are defined by the forms provided in Equations 4.2 to 4.4, the current can be rewritten as the sum of two sinusoids using trigonometric identities. One of these sinusoids is in phase with the voltage and is termed the real current. The other lags or leads the voltage by 90° and is termed the reactive current. When the voltage is at the zero crossing the real current is also at its zero crossing point, but the reactive current is at its peak value of $\sin(\theta)$. By calculating the peak value of the current during the zero

voltage point, it is then possible to solve for reactive power as shown in Equation 4.5. A phasor diagram representation for these calculations is provided in Figure 4.1.

$$v(t) = V\cos(\omega t) \tag{4.2}$$

$$i(t) = I\cos(\omega t - \theta) \tag{4.3}$$

$$i(t) = I(\cos(\theta) * \cos(\omega t)) + I(\sin(\theta) * \sin(\omega t)) \tag{4.4}$$

$$Q = V I * \sin(\theta) \tag{4.5}$$

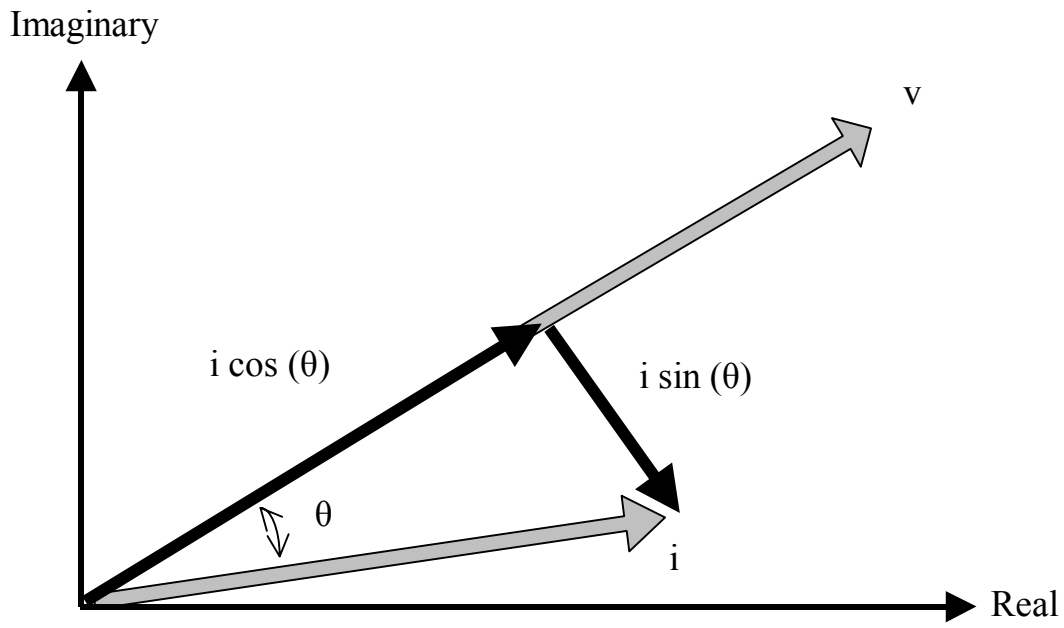

Figure 4.1: Phasor Diagram of Real and Reactive Current Components

It is important to note that the voltage crosses the zero axis twice per cycle, and the reactive current at these points are equal and opposite in magnitude. Recognizing that the zero crossing from negative to positive voltage corresponds to the opposite desired magnitude, the sign of the current magnitude at these points is negated. This convention is illustrated in Figure 4.2.

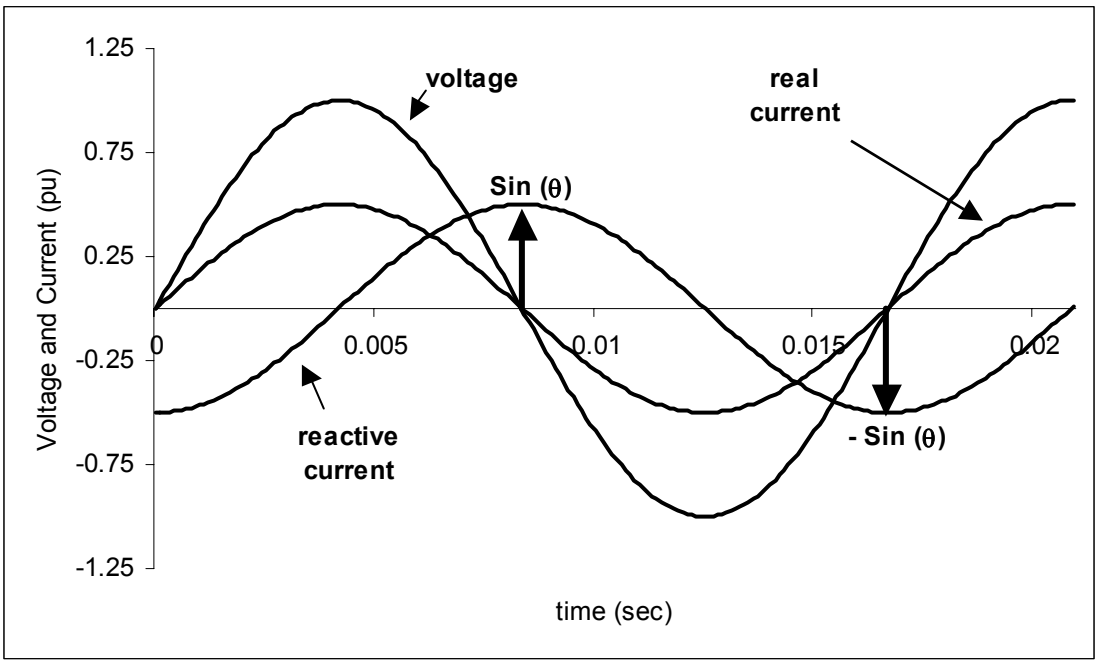

Figure 4.2: Reactive Current Magnitude Sign Convention

Phase Lock Loop Operation

Accurate measurement of the sin (θ) value is essential for correct application of the zero crossing algorithm. Small errors in sin (θ) value can result in significant errors in the reactive power and consequently too much or too little reactive power generation can be switched in by the controller.

Measurement of the reactive current peak from the unfiltered input is problematic. Without filtering, harmonics found in the signals will distort the wave shape of both voltage and current resulting in inaccurate measurements of reactive current. A phase lock loop (PLL) is proposed as a filtering method to eliminate these issues. Not only does a phase lock loop act as an excellent filter, it provides a constant sinusoidal output locked in quadrature with the input. Consequently, the output of a PLL is therefore ideal for measuring the reactive current magnitude. To insure accurate measurement of the reactive current, it is necessary to apply a phase lock loop to all current and voltage inputs into the controller. Not only does this filter out the harmonic content, it also keeps the phase shift equal among the inputs. The block diagram for the proposed PLL is presented in Figure 4.3.

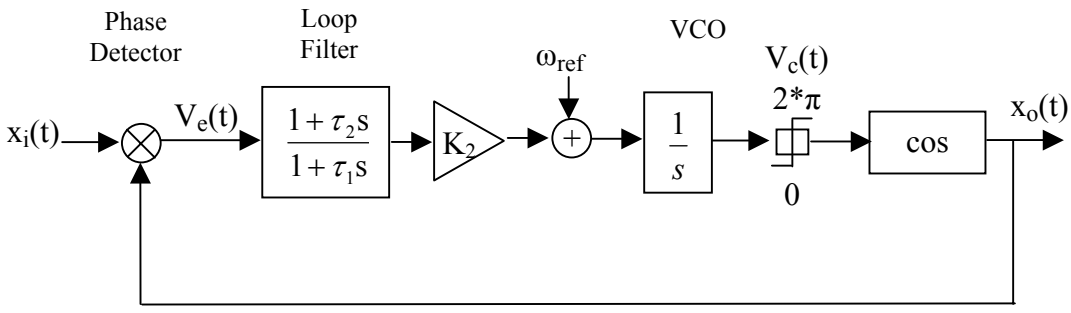

Figure 4.3: Model of a Phase Lock Loop

The phase detector component acts simply as a perfect multiplier of the input and feedback signals. If it is assumed at start up that the inputs to the multiplier share the

same frequency, the output of the phase detector will contain a frequency component at twice the input frequencies (ω) and a dc term as shown in Equation 4.8.

$$x_i(t) = A\cos(\omega t + \theta_i) \tag{4.6}$$

$$x_o(t) = B\cos(\omega t + \varphi_o) \tag{4.7}$$

$$v_e(t) = \frac{AB}{2}\left[\cos(2\omega t + \theta_i + \varphi_o) + \cos(\theta_i - \varphi_o)\right] \tag{4.8}$$

Assuming that loop filter is a perfect filter, it will remove the higher frequency component of v_e containing the 2nd harmonic term. The resulting signal is termed the control voltage and is defined by Equations 4.9 and 4.10.

$$V_c(t) = K_1\left[\cos(\theta_i - \varphi_o)\right] \tag{4.9}$$

$$K_1 = \frac{AB}{2} \tag{4.10}$$

If the phase detector inputs are initially in phase with each other, the control voltage will act on the VCO to increase the phase angle of the feedack signal until it is leading the input by a phase of 90°. At this point the PLL is said to be in lock with the input signal and the error voltage is zero. If the intial feedback signal lags the input signal signal by more than 90°, the control voltage will act on the VCO to decrease the angle of the feedback signal until lock of the signal is obtained. The operational principles that the PLL uses to obtain lock on the input signal are also what allow it to track the phase of the input signal. The relationship between the phases of the two inputs when locked is known as the phase qaudrature, and the φ_0 term is usually replaced with the relation $\theta_0 = \varphi_0 - \pi/2$, and the difference between the input phase angles, $\theta = \theta_i - \theta_0$,

is called the phase error. Figure 4.4 provides the block diagram for the developed voltage controlled oscillator.

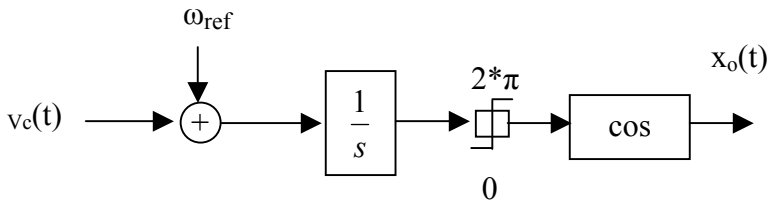

Figure 4.4: Functional Blocks of Voltage Controlled Oscillator

Equation 4.11 gives the VCO output in terms of the control voltage (v_c). If it assumed for the time being that v_c is a constant value 'x,' the effects of the control voltage on the output frequency are shown in Equation 4.12. Positive values 'x' work to increase the frequency of the output signal while negative values result in a decrease in frequency. The average value of v_c over time therefore increases or decreases the output frequency to reach lock and track the input's phase. Because the control voltage is intergrated over time, considerable changes in the control voltage during transients will help the PLL's ability to lock on and track the signal.

$$x_o(t) = \cos(\omega_{ref} t + \int_0^t V_c(t))dt \tag{4.11}$$

$$x_o(t) = \cos\{(\omega_{ref} + x)t\} \tag{4.12}$$

Integrating the control voltage over an ever increasing amount of time results in an ever increasing value. While this is not a problem mathematically as shown in Equation 4.11, calculating this value in software would eventually cause a numerical overflow error. In order to alleivate this possibility, the output of the integrator is reset to zero after reaching a full period of 2π. This restricts the numerical size of the integrated control voltage without affecting the output of the VCO. The resulting saw tooth shaped signal provides an easy method of evaluating the operation of the PLL, because the rate at which the average rises to 2π directly results in the frequency the VCO outputs. An example of the saw tooth shaped average produced during start up with an in-phase reference is presented in Figure 4.5. The PLL first acts to increase the frequency of its output, overshoots this value, and then acts to decrease the frequency output until lock is achieved. Lock is easily noted as the point when the sawtooth value is zero at the same time as the negative to postive zero crossing of the input signal.

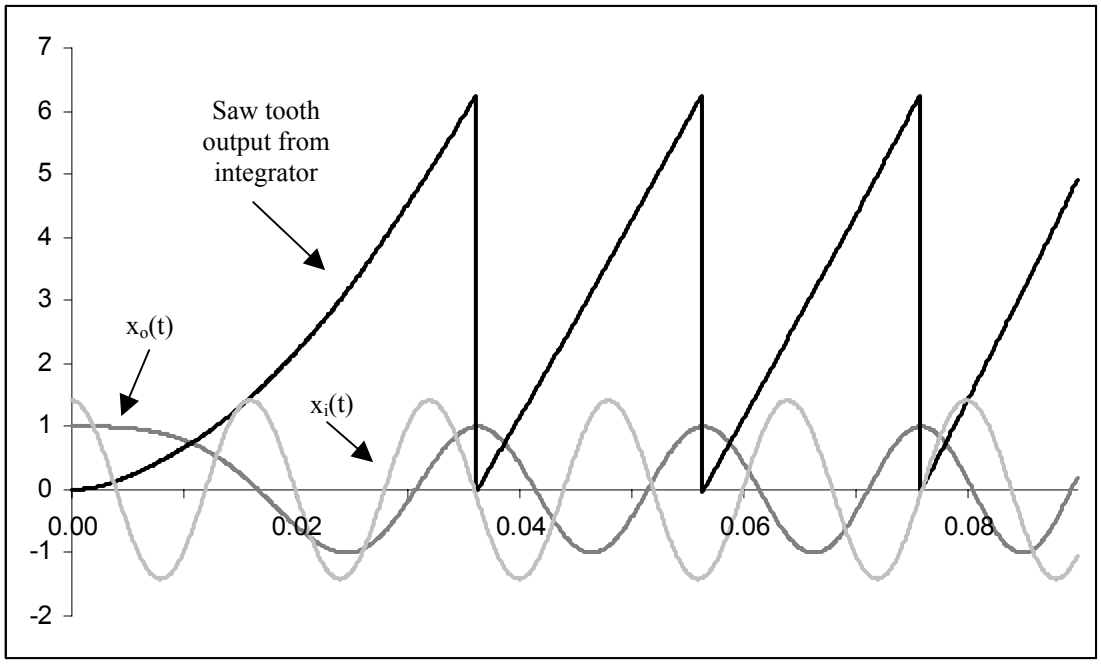

Figure 4.5: Example of PLL Frequency Adjustment

Phase Lock Loop Optimization

Optimization of the phase lock loop is essential for correct response to various waveforms of current and voltage, and the PLL is optimized through the loop filter. Previously the loop filter was assumed to be a perfect low-pass filter and had a minor role in the operation of the PLL. In actuality, the characteristics of the loop filter are an integral part of the operation and stability of the phase lock loop. In this case, the proposed PLL model utilizes a lag-lead controller for the loop filter, which exhibits better filtering characteristics than a PI controller [7] while providing better stability than a low-pass filter.

While the operation of the PLL is non-linear of a linear system, when the phase error is low the operation of the PLL is sufficiently linear to model for stability purposes.

During linear operation of the PLL, the phase detector and the VCO can be simplified as simple gains in the feedback loop [8]. The loop now consists of a loop gain (K), the loop filter, and an integrator. Given that the loop is linearized, the PLL is only affected by changes in phase, and the input and output terms can be redefined as $\theta_i(s)$ and $\theta_0(s)$ respectively. Figure 4.6 shows the simplified model of the linearized PLL. The resulting transfer function, using a lag-lead controller, is defined in Equation 4.14.

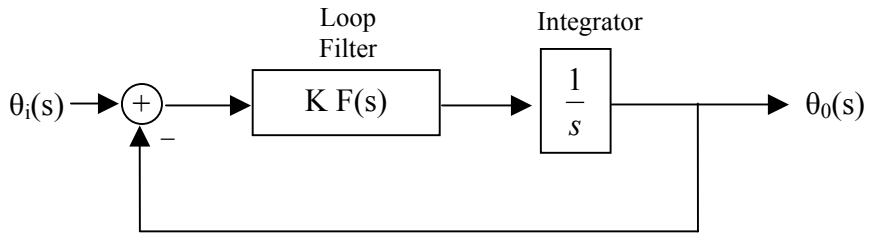

Figure 4.6: Linearized Phase Lock Loop Model

$$F(s) = \left(\frac{1 + s\tau_2}{1 + s\tau_1}\right)K_2 \tag{4.13}$$

$$H(s) = \frac{\theta_0(s)}{\theta_i(s)} = \frac{KF(s)}{s + KF(s)} = \frac{K(\tau_1 s + 1)}{\tau_1 s^2 + (1 + K\tau_2)s + K} \tag{4.14}$$

$$K = K_1 * K_2 * K_3 \tag{4.15}$$

where

F(s) = Loop filter transfer function

K = Loop gain

K_1 = Phase detector gain

K_2 = Loop filter gain

K_3 = VCO modulation sensitivity

The phase detector gain is taken directly from Equation 4.9, and the loop filter gain is a design value for the lag-lead controller. The VCO modulation sensitivity is a measure of the change in frequency per change in the control voltage and can be explained using Equation 4.11. For example, if $v_c(t)$ is set to a constant value equal to the reference frequency (ω_{ref}), the frequecy of $x_0(t)$ will be $2*\omega_{ref}$. Any constant value selected for $v_c(t)$ results in a change of frequency equal to the value given for $v_c(t)$. Therefore for the given VCO, a change in v_c corresponds to an equal change in the VCO modulation and K_3 is equal to one. This relationship is mathematically defined in Equation 4.16.

$$\frac{d\theta_0}{dt} = K_3 Vc \tag{4.16}$$

Two important values when designing the PLL are the damping ratio (ζ) and the natural or undamped frequency (ω_n). The values are derived from the transfer function and by definintion are:

$$\omega_n = \sqrt{\frac{K}{\tau_1}} \tag{4.17}$$

$$\xi = \left[\frac{1 + K\tau_2}{\tau_1}\right]\left[\frac{1}{2\omega_n}\right] \tag{4.18}$$

The importance of these values with respect to input phase changes can be explained by developing the error function of the loop in terms of the step in phase of the input. The error function is defined as 1-H(s) and is given in Equation 4.19 for a PLL with a lag-lead filter. The term $\theta(s)$ was defined earlier as the phase error or the difference between the input and output signal phases.

$$1 - H(s) = \frac{\theta(s)}{\theta_i(s)} = \frac{s}{s + KF(s)} = \frac{s^2 + (\omega_n^2/K)s}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{4.19}$$

Equation 4.20 represents the input phase angle when, at t = 0, a step in phase of magnitude ϕ is applied, where $u(t)$ is the unit step function. Using the Laplace transformation, Equation 4.20 can be rewritten and substituted into Equation 4.19 to solve for the phase error.

$$\theta_i(t) = \phi\, u(t) \tag{4.20}$$

$$\theta(s) = [1 - H(s)]\frac{\phi}{s} = \frac{(s + \omega_n^2/K)\phi}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{4.21}$$

If the denominator is broken down into a $(s+\alpha)(s+\beta)$ relation and the inverse Laplace transform is taken, Equation 4.21 can be solved as a function of time for $\xi > 1$ [9].

$$\theta(t) = \phi e^{-\xi\omega_n t}\left[\cosh\left(\omega_n\sqrt{\xi^2-1}\,t\right) + \left(\frac{\omega_n/K-\xi}{\sqrt{\zeta^2-1}}\right)\sinh\left(\sqrt{\xi^2-1}\,t\right)\right] \qquad (4.22)$$

Equation 4.22 provides a way to quantify the error in the output phase with step changes in the input phase over a period of time. Choosing constant values for τ_1 and τ_2, the pole and zero of the lag-lead controller, the value of *K* will have direct influence on the magnitudes of the damping ratio and natural frequency. Figure 4.7 shows that the higher the value of K the quicker the phase error will be minimized. Increases in the gain K, however, will decrease the ability of the loop filter to minimize the 2nd harmonic, as shown in Equation 4.8. In order to insure effective switching of the capacitors in the compensator, it is necessary to have as minimum an error as possible after one cycle or 16.667 ms. The K value is selected so that the error is minimal after one cycle, but for higher values of K the ability of the loop filter to filter out harmonic content is diminished.

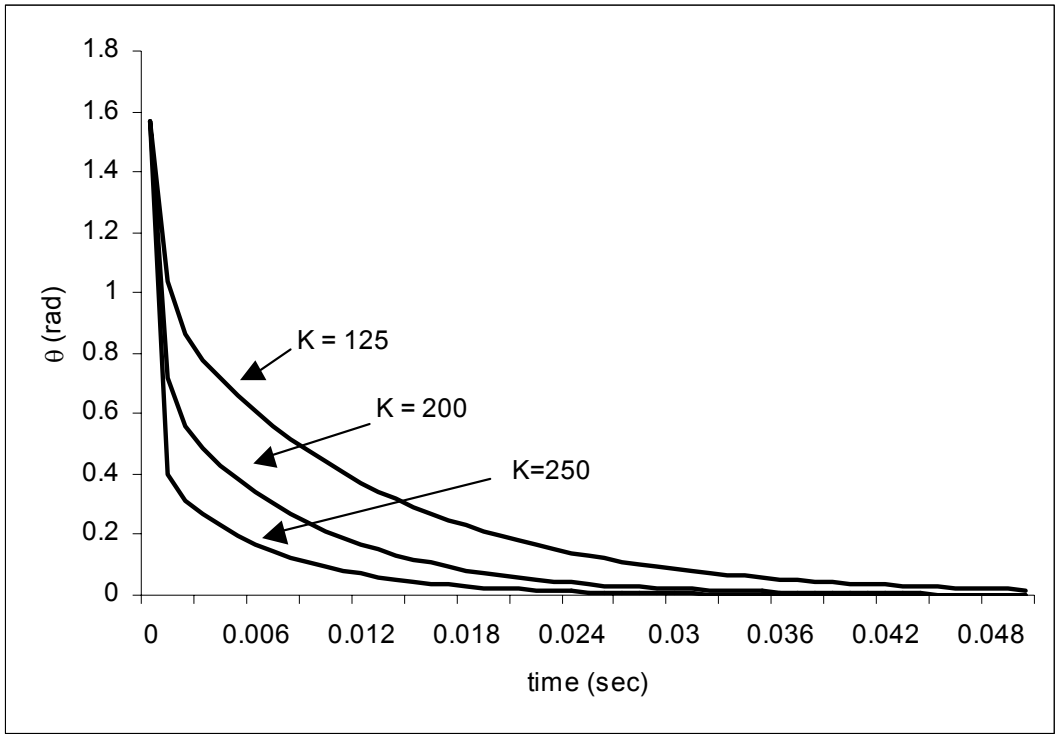

Figure 4.7: Phase Error Plots for Three Cycles with π/2 Phase Step
($\tau_1 = 0.001$ & $\tau_2 = 0.005$ sec)

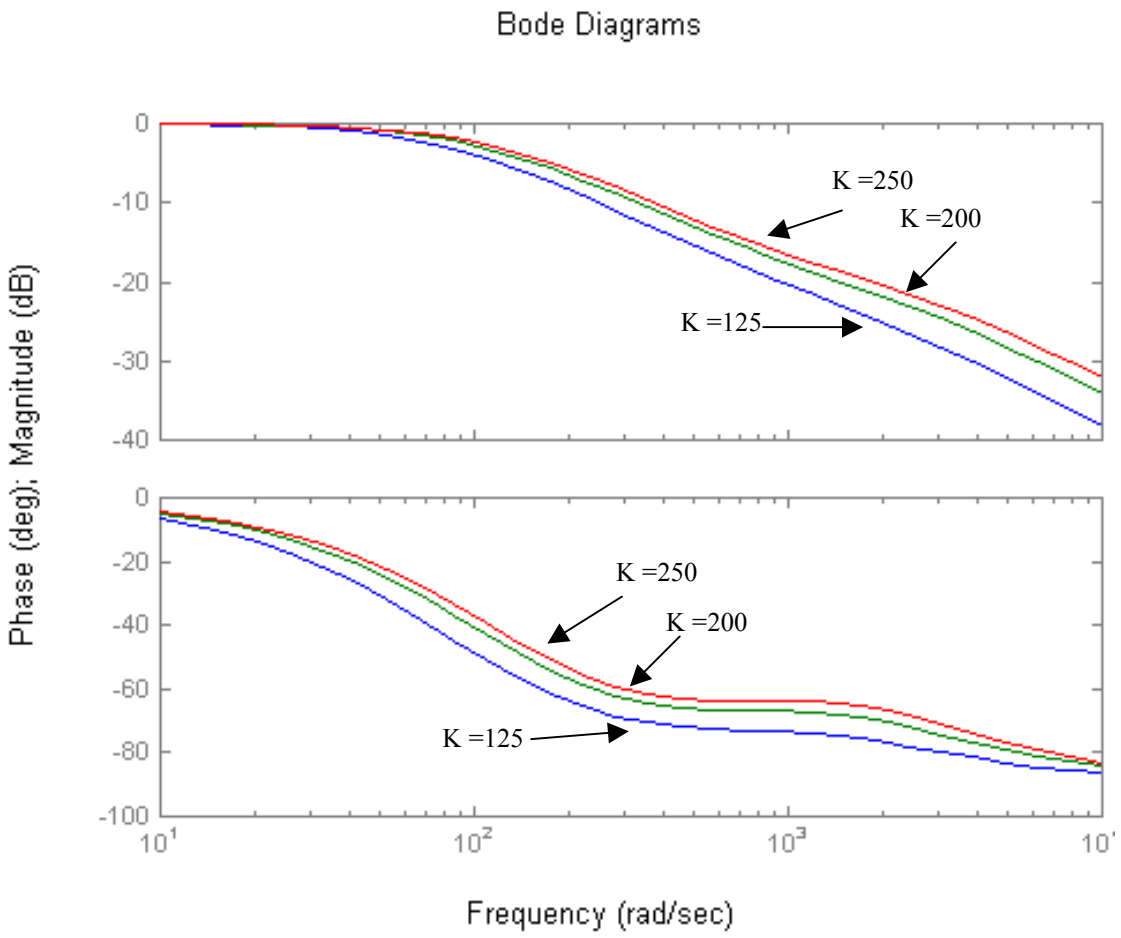

Figure 4.8: Bode Plots for Loop Gain Values

The phase lock loop models used for the voltage and current calculations share the same design for the lag-lead filter, but different values for the loop filter gain are required. This is an effort to keep the loop gains of both PLLs relatively equal during nominal operating conditions. Because the voltage phase and magnitude are held relatively constant by the power system, the PLL can be designed to effectively limit the voltage harmonics by using a low value for the loop gain. The phase and magnitude of current waveforms, however, are constantly changing with the load. Higher values of

current magnitude will result in an increase of the loop gain by increasing the phase detector gain. As shown, increases in the value of K help the PLL respond quickly to phase changes, but decrease the ability of the loop filter to handle harmonic content. The inability to handle harmonic content is a significant factor when applying a mitigation device at industrial locations. While the operation of the PLLs are dependant on the magnitude of the input signals for their filtering abilities, the least squares algorithm applies filtering methods that are not so directly affected by these magnitudes.

Least Squares Method

The least squares approach is a method that allows for the direct estimation of the current and voltage magnitudes and angles. The reactive power can be directly calculated from these values without the necessary techniques involved with measuring the zero crossing value. The least squares method also can be used with as little as three samples at a time. This property of the method allows for a more frequent determination of the reactive power at higher sampling rates.

Supposing that any sinusoidal signal can be broken down into real and reactive components, as previously discussed for the zero crossing method, Equation 4.4 then can be rewritten in a manner independent of the type of source.

$$y(t) = Y_r \cos(\omega t) + Y_i \sin(\omega t) \tag{4.23}$$

Therefore, at any point in time the value of y(t) is equal to the sum of the real and imaginary components.

Figure 4.9 provides a diagram of the sampling process used by the least squares method. If the most recent sample is defined to be the point where the real component is at its maximum and the imaginary component is zero, the previous samples can be related by the fundamental frequency angle between samples (Φ), where the fundamental frequency angle is the fixed time interval between samples multiplied by the frequency of the power system, or $\Phi = \Delta t * \omega$. The relationship between the sample and the component magnitudes is given in Equation 4.24 for three samples.

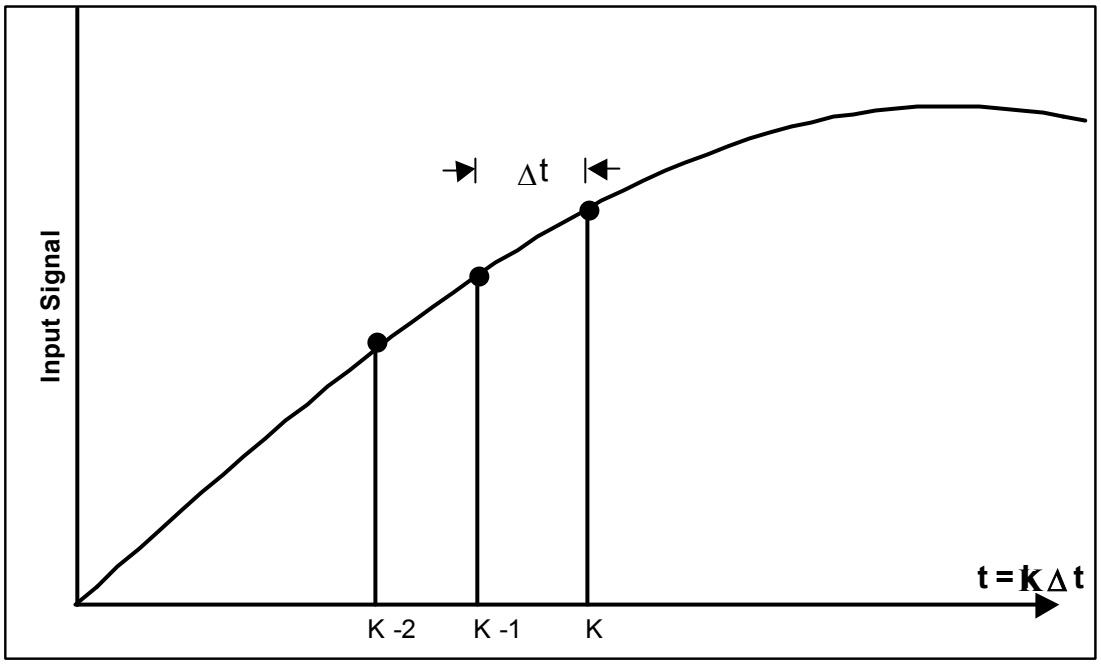

Figure 4.9: Least Squares Method Sampling Relationship

$$\begin{bmatrix} Y_{K-2} \\ Y_{K-1} \\ Y_K \end{bmatrix} = \begin{bmatrix} \cos(2\Phi) & -\sin(2\Phi) \\ \cos(\Phi) & -\sin(\Phi) \\ 1 & 0 \end{bmatrix} \begin{bmatrix} Y_r \\ Y_i \end{bmatrix} \tag{4.24}$$

Using three samples overdefines the relationship as there are two unknowns and three equations, but the extra equation is employed to provide some immunity to variations in the signal. Equation 4.24 is solved using the method of least squares. Equations 4.25 to 4.27 show how the least squares method is applied to an overdetermined set of linear equations.

$$\bar{b} = [A]\,\bar{x} \tag{4.25}$$

$$[A]^T[A]\bar{x} = [A]^T\,\bar{b} \tag{4.26}$$

$$\bar{x} = \{[A]^T[A]\}^{-1}[A]^T\,\bar{b} \tag{4.27}$$

The constant sampling rate defines the constant value for the fundamental frequency angle. Consequently, the relation between the sample values and the values of Y_r and Y_i can be evaluated prior to sampling by solving the matrix relation (4.27) in software for the chosen fundamental frequency angle. With the calculated values Y_r and Y_i, the magnitude and angle of the signal are established by transforming Equation 4.23 into its phasor representation.

$$|Y| = \sqrt{(Y_r)^2 + (Y_i)^2} \tag{4.28}$$

$$\theta_y = \tan^{-1}\left[\frac{Y_i}{Y_r}\right] \tag{4.29}$$

The angles provided by Equation 4.29 will rotate with each sample point by the fundamental frequency angle Φ [9]. The resulting change in angle, however, is applied equally to both the voltage and current calculations and will cancel out when the difference between the two angles is calculated.

Assuming a 600 Hz sampling rate, Table 4.1 provides sampled data from a 60 Hz voltage source with a magnitude of 1 Vrms. The relation between the sampled data and the Y_r and Y_i values is given as:

$$\Phi = \Delta t * \omega = \frac{1}{600} * (2\pi * 60) = \frac{\pi}{5}$$

$$\begin{bmatrix} Y_{K-2} \\ Y_{K-1} \\ Y_K \end{bmatrix} = \begin{bmatrix} \cos(2\pi/5) & -\sin(2\pi/5) \\ \cos(\pi/5) & -\sin(\pi/5) \\ 1 & 0 \end{bmatrix} \begin{bmatrix} Y_r \\ Y_i \end{bmatrix}$$

Using the least squares relation given in Equation 4.27, the matrices can be rewritten to solve directly for Y_r and Y_i.

$$\begin{bmatrix} Y_r \\ Y_i \end{bmatrix} = \begin{bmatrix} -0.2165 & 0.3504 & 0.7835 \\ -0.8941 & -0.2546 & 0.4822 \end{bmatrix} \begin{bmatrix} Y_{-2} \\ Y_{-1} \\ Y_0 \end{bmatrix}$$

This relationship can then be used to solve for real and imaginary components with any three sequential points sampled from a signal at 600 Hz. The real and imaginary component results along with their polar transformations are provided in Table 4.1. Note that the angle of the results changes by the fundamental frequency angle for each set of calculations.

Table 4.1

Least Squares Example Data

time	Y_k	Y_r	Y_i	Magnitude	Angle (rad)
0.0000	1.2247				
0.0017	1.4065				
0.0033	1.0509	1.0509	-0.9463	1.4143	-0.7331
0.0050	0.2940	0.2940	-1.3833	1.4142	-1.3614
0.0067	-0.5753	-0.5753	-1.2919	1.4142	-1.9897
0.0083	-1.2248	-1.2248	-0.7070	1.4142	-2.6181
0.0100	-1.4065	-1.4065	0.1480	1.4142	3.0368

However Equation 4.23 does not contain any harmonic terms and any harmonics present would result in error in the solution for Y_r and Y_i. To minimize the effects of harmonics in the calculations, a 4th order Butterworth filter is first applied to the sampled data before the least squares estimation. The transfer function for the 4th order Butterworth filter used is given in Equation 4.30. A cutoff frequency of $\omega = 753$ rad/sec was selected for the filter. As shown in Fig 4.10, this value for the cutoff frequency provides filtering for high harmonic content with little attenuation of the fundamental frequency.

$$H(s)_{\text{Butterworth}} = \frac{\omega^4}{(s^2 + 0.765s\omega + \omega^2)(s^2 + 1.85s\omega + \omega^2)} \tag{4.30}$$

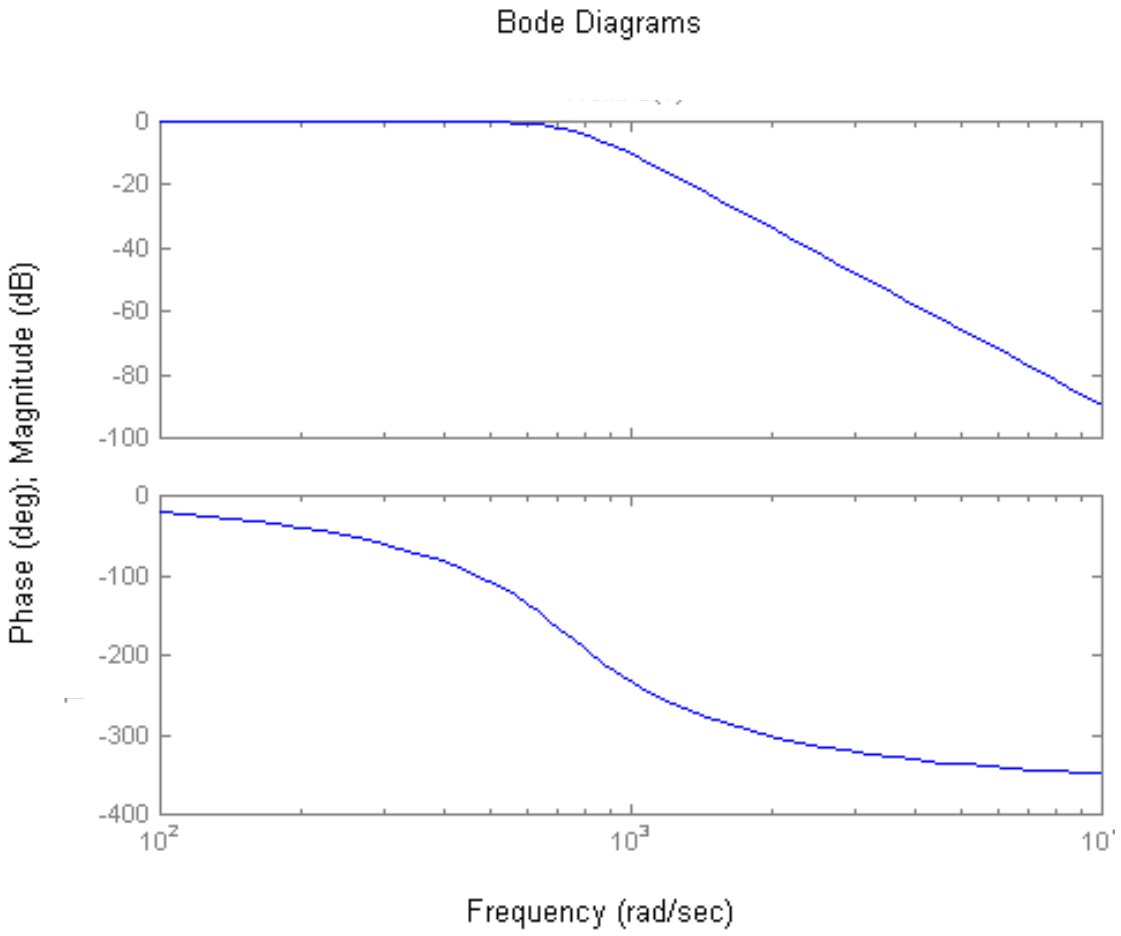

Figure 4.10: 4th Order Butterworth Filter Bode Plot

The output from the Butterworth filter is applied to the least squares algorithm to calculate the reactive power. Errors in the least squares solution will show up as 120 Hz ripples in the output, which can then be filtered using a low-pass filter. The application of the low-pass filter is possible because at steady state the reactive power is a constant DC value. Because both filters require time to settle after changes in the input signal, the low-pass filter is optimally designed to provide the highest filtering capability while

keeping the total settling time of both filters below one cycle. The s-domain transfer function of the low-pass filter is given in Equation 4.31 along with the Bode response in Fig. 4.11. Through simulation of the least squares algorithm, it was found that a value of $\tau_1 = 0.003$ provides the best filtering capabilities while still keeping the settling time of the algorithm within one cycle.

$$H(s)_{Lowpass} = \frac{1}{1 + s\tau_1} \tag{4.31}$$

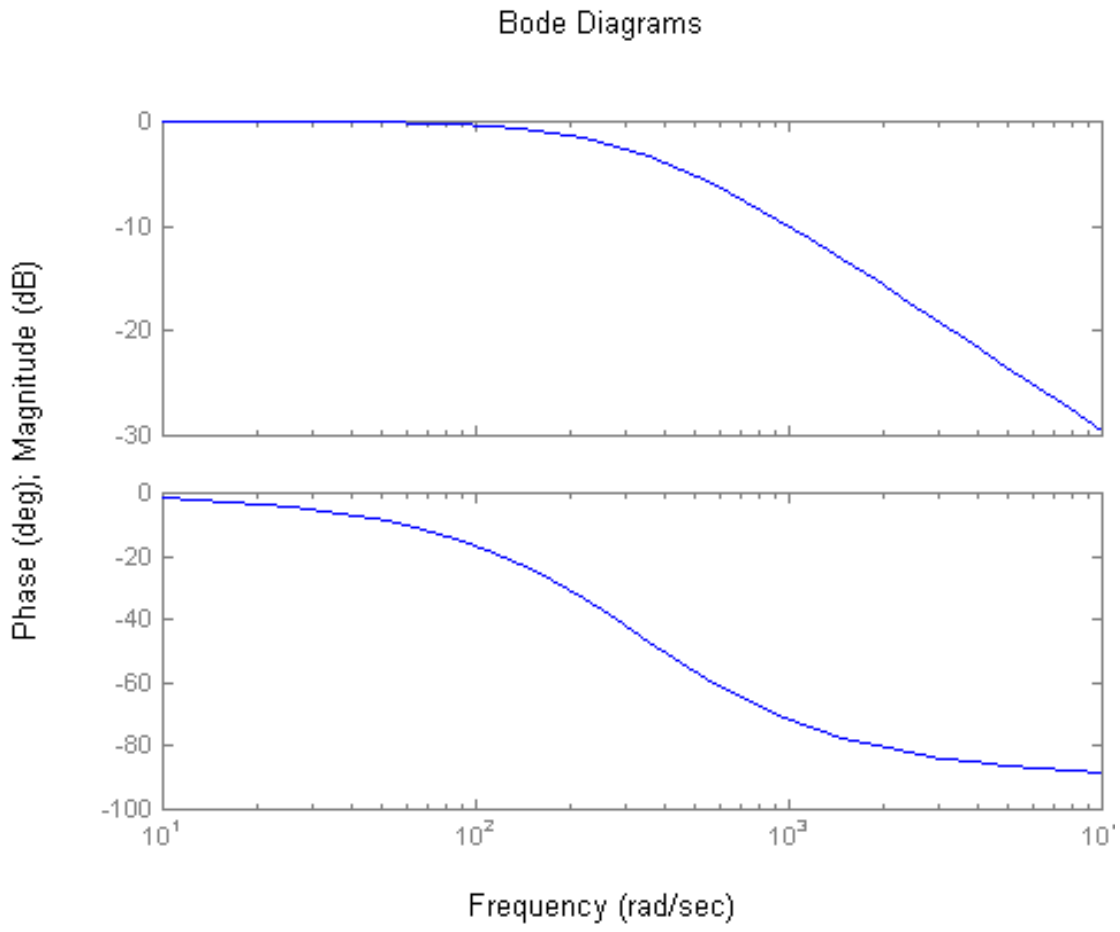

Figure 4.11: Low-pass Filter Bode Plot

While the Butterworth and low-pass filters are capable of removing large amounts of harmonic content and error in the reactive power calculation, the fundamental frequency angle also has a significant role in the least squares algorithm's ability to isolate the fundamental frequency from the harmonic content and other variations. As the sampling rate increases the fundamental frequency angle decreases and more of the harmonic content is sampled. Because the least squares method provides a curve to best fit the data points, a higher number of sampled harmonic points will result in the method fitting the curve to fundamental frequency with any remaining harmonic content showing up as error. When more of the harmonic content is sampled the least squares method sees the harmonic content as part of the signal and not as variances in the signal, and this results in error in the reactive power calculations. Therefore a low sampling rate will provide better harmonic limiting capabilities and as a result less error in the calculations. While using low sampling rates will eliminate some the calculation error, care should be made not to lower the sampling rate beyond the smallest time constant of the filtering devices.

Insuring that the sampling rate is significantly higher than the smallest time constant insures the accuracy and numerical stability of the calculations. Because the time constant of the filter is a measure of the signal ability to change rapidly, if the sampling rate is low relative to the time constant the filter will be limited in its ability to track changes in the signal. Consequently, stability and accuracy will be jeopardized. The smallest time constant for the filters is found in the Butterworth filter and has a value of 1.4338 ms. Therefore to maximize stability and accuracy of the least squares method

the sampling rate must be higher than 700 Hz. However the sampling rate cannot be increased too high because then the processor cannot complete the calculations in real time. Therefore a trade off between accuracy and calculation time must be made.

Evaluation of Proposed Methods

The proposed methods for calculating the reactive power must be able to respond quickly and accurately to reactive power demand changes. The ability of the proposed algorithms to provide accurate and quick results was tested through simulation. The previously developed parameters for the PLL and least squares filters are given in Table 4.2. The input functions for the simulation are given in Equations 4.33 to 4.35. The current input consists of the fundamental frequency and a 3rd harmonic. This simulation assumes that the 3rd harmonic is 30% of the fundamental, and at t = 0.2 seconds, a reactive load is introduced. At this point, the 60 Hz rms current is increased from 0.2 pu to 1.0 pu with the worse case phase shift of 90° applied immediately at the switching point. The graphical representation of this input is given in Figure 4.12.

$$v(t) = 1\sqrt{2}\sin(2\pi 60\,t) \tag{4.33}$$

$$i(t) = 0.2\sqrt{2}\sin(2\pi 60\,t) + 0.2\sqrt{2}\sin(3 * \pi 60\,t) \tag{4.34}$$

for t > 0.2 seconds:

$$i(t) = 1\sqrt{2}\sin(2\pi 60\,t + 90°) + 0.2\sqrt{2}\sin(3 * (\pi 60\,t - 90°)) \tag{4.35}$$

Table 4.2

PLL & Least Squares Method Parameters

Zero Crossing		**Least Squares**	
$T_{1(Lag\text{-}Lead)}$ (sec)	0.005	$\Omega_{(Butterworth)}$ (rad/s)	754
$t_{2(Lag\text{-}Lead)}$ (sec)	0.001	$T_{1(low\text{-}pass)}$ (rad/s)	0.003
$K_{2Voltage}$	250		
$K_{2Current}$	50		

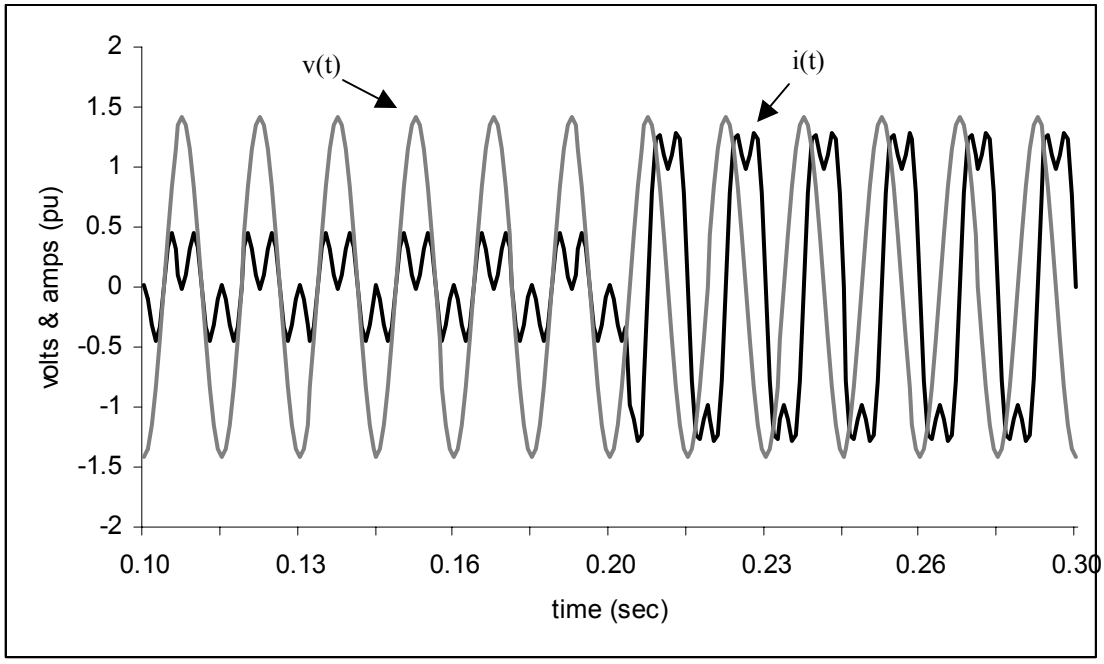

Figure 4.12: Test Voltage and Current Input

Figure 4.13 shows the response of both algorithms to the given input. The effects of the third harmonic are easily seen in the least squares method, but are not so obvious for the zero crossing method. Examining the error in the zero crossing method before the t = 0.2 point, the voltage and current PLLs were designed to have the same loop gain, where $K_{current} = 0.2 * 250 * 1.0 = 50$ and $K_{voltage} = 1.0 * 50 * 1.0 = 50$. Nonetheless, this does not take into account the diminished capability of the loop filter to reduce the harmonic content of the input due to the higher loop filter gain. Consequently, the unfiltered harmonic content appears as a change in the phase detector gain. Examining Equation 4.19, two PLLs with differing values of K will have different values for the phase error θ. The difference in the phase error shows up then as error in the imaginary current component measurement. The error after switching of the reactive load is not as apparent because the *di/dt* values are not as high about the voltage zero crossing point when the current is shifted by 90º.

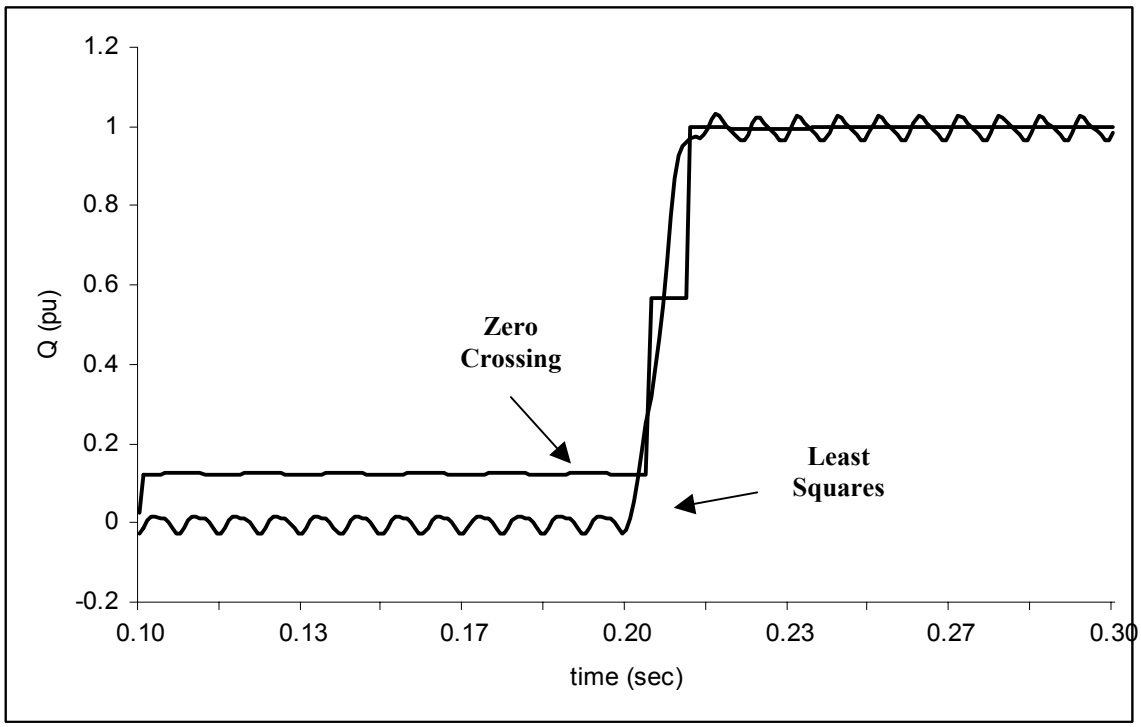

Figure 4.13: Response to an Increase in Reactive Demand and 3rd Order Harmonic

The inability of the zero crossing method to handle different values of *K* is extremely apparent when changes in current magnitude are applied with small or no changes in phase, specifically the application of resistive loads. The calculated reactive power provided in Figure 4.14 for both methods when a purely resistive load is applied to the system without the third harmonic. In this case, the equations used are the same as those given in Equations 4.33 to 4.35 except the angle of the current is not shifted at the t =0.2 point as given in Equations 4.36 to 4.38. While the zero crossing method provides better immunity to harmonic content than the least squares method, clearly the response of the zero crossing method is such that it will not accurately calculate the reactive power demand under all conditions. At least as considered here, the zero crossing method is not

an applicable one for calculating the reactive power demand in order to control the switching of the proposed TSC.

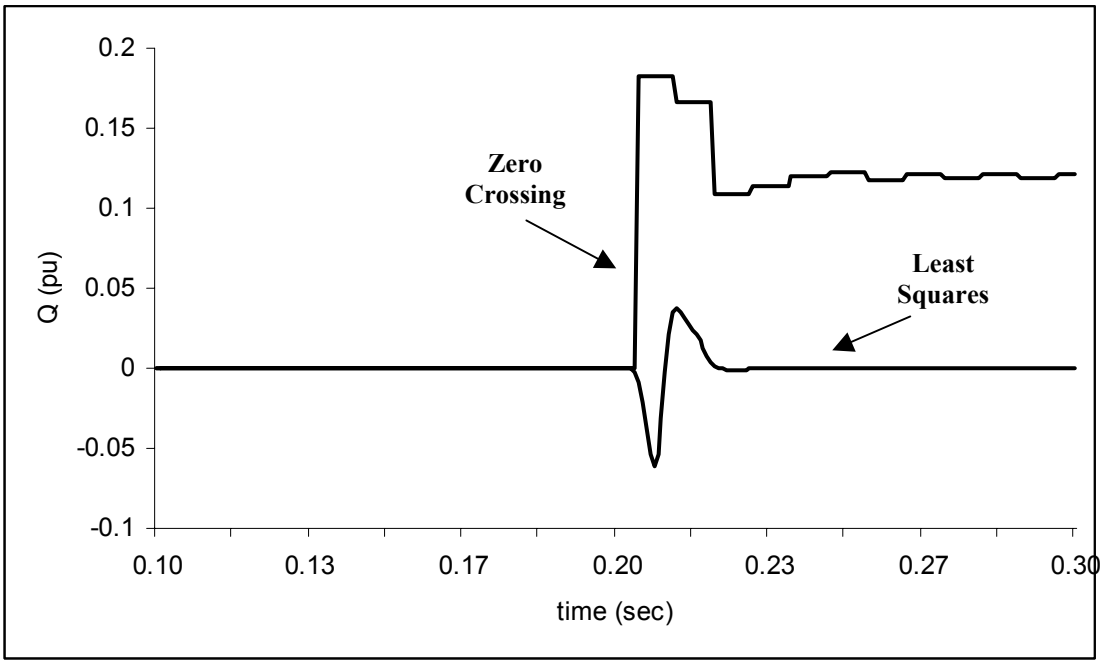

Figure 4.14: Response to Current Magnitude Change and 3rd Order Harmonic

$$v(t) = 1\sqrt{2}\sin(2\pi 60\,t) \tag{4.36}$$

$$i(t) = 0.2\sqrt{2}\sin(2\pi 60\,t) + 0.06\sqrt{2}\sin(6\pi 60\,t) \tag{4.37}$$

at $t > 0.2$ seconds:

$$i(t) = 1\sqrt{2}\sin(2\pi 60\,t) + 0.06\sqrt{2}\sin(6\pi 60\,t) \tag{4.38}$$

While the least squares method is not as efficient as the PLLs at filtering out the harmonic content of the waveforms, it is still an effective means of curtailing the error in

calculating the reactive power demand. Table 4.3 gives a worst-case scenario for harmonic content using the harmonic limits set by IEEE Std. 519-1992 [10]. Using Equations 4.33 to 4.35 with the added harmonic content of Table 4.3, the results from the least squared algorithm are given in Fig. 4.15 with a sampling rate of 960 Hz. This figure clearly shows that the least squares method is an effective means for calculating an accurate value for the reactive power demand with a small relative error. The effects of the relative error on overall compensator performance, however, cannot be evaluated without first examining the logic used to determine the discrete value of the reactive power to be switched in the circuit.

Table 4.3

Worst Case Harmonic Content

	V	I
Fundamental	100.00%	100.00%
2nd Harmonic	0.75%	3.75%
3rd Harmonic	3.00%	15.00%
4th Harmonic	0.75%	3.75%
5th Harmonic	3.00%	15.00%
10th Harmonic	0.75%	3.75%
11th Harmonic	3.00%	7.00%
12th Harmonic	0.75%	1.75%
13th Harmonic	3.00%	7.00%

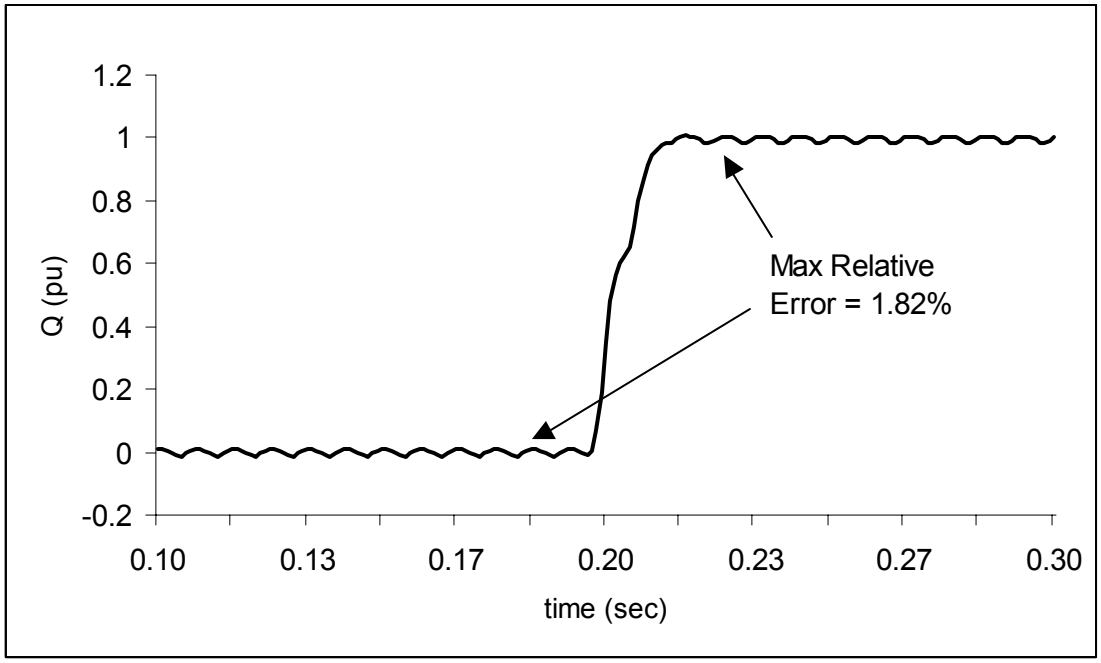

Figure 4.15: Least Squares Results at 960 Hz Sampling Rate

Capacitor Switching Algorithm

Assume that there are N capacitors in the binary ratio configuration (Q_N, Q_{N-1}, …Q_1) with Q_N as the largest. Defining a value $Q_{1/2}$ as half the kvar value of the smallest capacitor, the reactive power measured (Q_M) is first compared to the largest capacitor rating. If the measured value is larger than the rating of Q_N minus $Q_{1/2}$, then a gating signal is sent to the capacitor's gate control circuit and the rating of the capacitor is subtracted from reactive power measured quantity. If the measured value, Q_M, is smaller than Q_N, any existing gating signal for Q_N is removed. This procedure continues with the decreasing capacitor sizes until the smallest is reached. Equation 4.36 provides the

logical algorithm for these steps. Symbolically, the index N is reduced and the algorithm re-applied for the next smaller capacitor size until the smallest size is reached.

$$\begin{aligned} &\text{If}\left[Q_M \geq Q_N - Q_{1/2}\right] \\ &\qquad Q_M = Q_M - Q_N \\ &\qquad \text{Gate } Q_N \\ &\text{Else} \\ &\qquad \text{Remove } Q_N \text{ Gate} \end{aligned} \tag{4.36}$$

The smallest rated unit is gated or not depending on if the remaining value of Q_M is larger than half the step size. Switching the capacitors in this manner permits a maximum reactive power supply deviance from the measured reactive demand of half the smallest unit. Figure 4.16 shows that using capacitor sizes of 10, 20, and 40 kvar the reactive power supplied will differ from the reactive power demand by no more than a maximum of 5 kvar, or half the smallest unit.

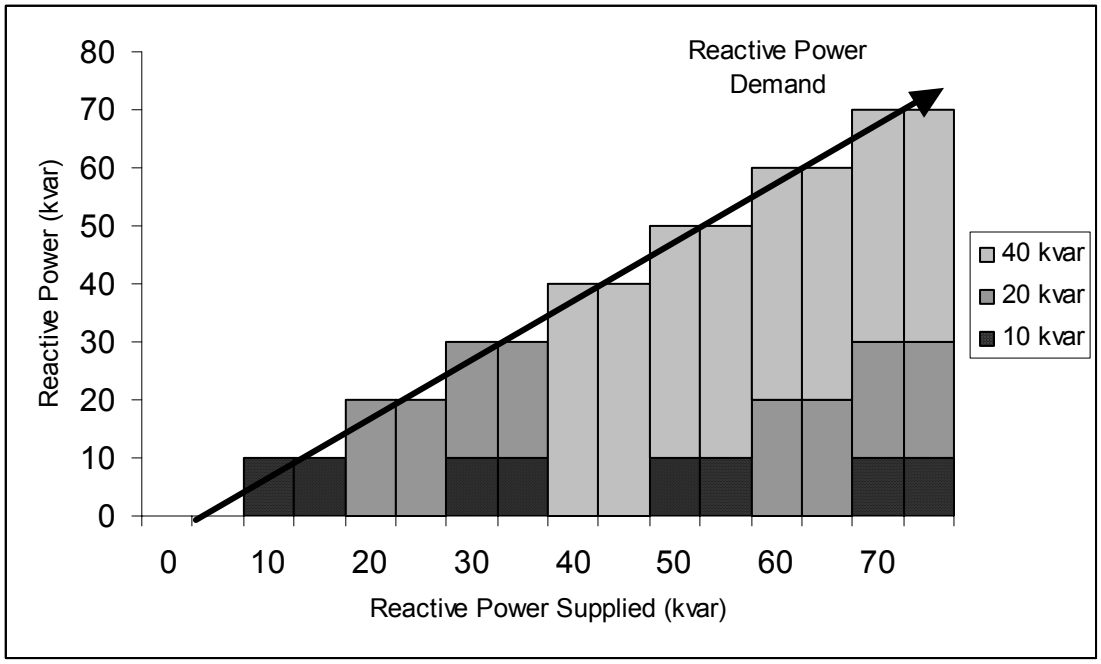

Figure 4.16: Example of Capacitor Switching Algorithm

The relative error produced by the least squares method can now be evaluated by examining the percent error required to switch in reactive power generation greater than one step from the reactive power demand. If we assume that the TSC has four capacitor banks sized by binary multiples, then the TSC will have 15 steps of reactive power. Therefore, each step corresponds to 6.67 % of the total reactive power capability of the unit, and a half step 3.33% of the capability. Because there is an inherent maximum error of a half step from the capacitor switching algorithm, the error from the least squares method must be added to the capacitor switching algorithm error. Therefore a relative error greater than a half step would create the potential for the TSC to be off in reactive power generation by a whole step. Therefore the error in the least squares method must be limited to half the percentage of the smallest step of the TSC. As shown in Figure 4.15

the maximum relative error for 960 Hz sampling is 1.82% and well within the error bounds to keep the total error less than a whole step in reactive generation.

CHAPTER V

APPLICATION AND ASSESSMENT

Assessment of the proposed TSC was accomplished by construction of a prototype with all the components physically implemented and the PC-104 controller operating in real time. This prototype provides an evaluation of the design's ability to supply reactive power for a widely varying load, in this case an induction motor. The reactive generation for each phase consists of four capacitors configured in the binary arrangement, with the smallest step size providing 54.3 var at rated voltage (120 V). Therefore each phase of the TSC will provide 15 steps of reactive generation up to a total of 814.5 var. Each capacitor was controlled by an individual gating circuit, IGBT module, and output signal from the PC-104 controller. The PC-104 controller was set to sample at a frequency of 700 Hz and to apply the switching algorithm every ¼ of a cycle. Note that faster processors would permit higher sampling rates if required. This arrangement offers a means of evaluating the operation of the components of the designed TSC as well as the methodologies behind the design.

The performance of the TSC was evaluated by collecting data on the reactive power demand of two induction motors and the reactive generation response by the TSC. The nameplate data for the motors is given in Table 5.1 and an example of the total real and reactive power consumption of the motors during start up is shown in Figure 5.1.

Table 5.1

Induction Motor Nameplate Data

	Wound Rotor	Squirrel Cage
Phase	3	3
hp	1/4	1/4
r/min	1500	1670
Volts	208	208
Amps	1.3	1.2
Hz	60	60

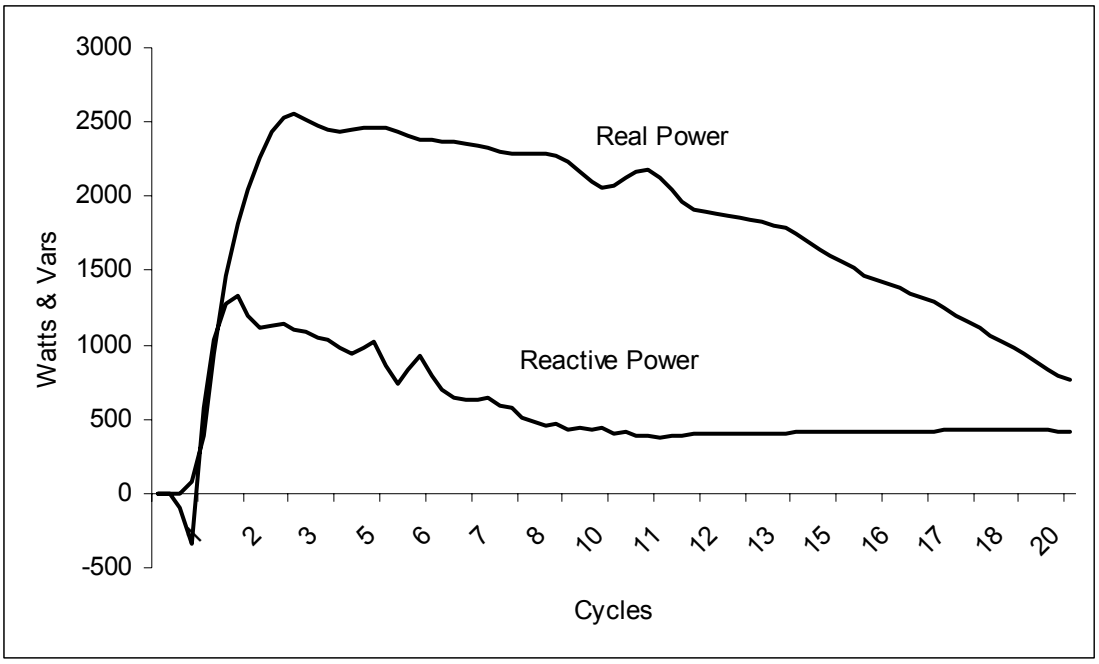

Figure 5.1: Real and Reactive Power Consumption of an Induction Motor Load During Start-up

Data was gathered using an independent data acquisition method that would not affect the performance of the TSC while still providing the necessary measurements for the calculation of the reactive power demand and generation. Because of the harmonic content found in the current signal, direct calculation of the reactive power supplied by the capacitors is not possible without filtering of the signal. Filtering of the signal is

achieved by a program similar to the one used by the controller. This program provides the same calculations as that of the controller but reads the sampled points in from a text file instead of from the data acquisition card while outputting the switching logic and reactive power values out to a text file. This will provide the necessary filtering of the currents while also providing a way of examining the behavior of the TSC as it responds to the motor start.

The measured voltage and currents for the first four cycles after the inductive motor load is switched in are shown in Figures 5.2, 5.4, and 5.6. As designed, switching of the capacitors is only taking place when the voltage is at the transient free switching point. The calculated reactive generation and reactive demand from the measured voltage and current quantities are diagramed in Figures 5.3, 5.5, and 5.7. One consequence of filtering the signals is the distortion of the step response in the reactive generation due to the settling times of the filters. To keep the step response reference distinguished, the output of the switching logic is also given in the following figures. One point to note is that the switching logic output shown is still subject to the timing provided by the gating circuit. Therefore changes in the switching logic output will not necessarily correspond to quick changes in the reactive generation because actual IGBT switching does not occur until a voltage minimum is reached.

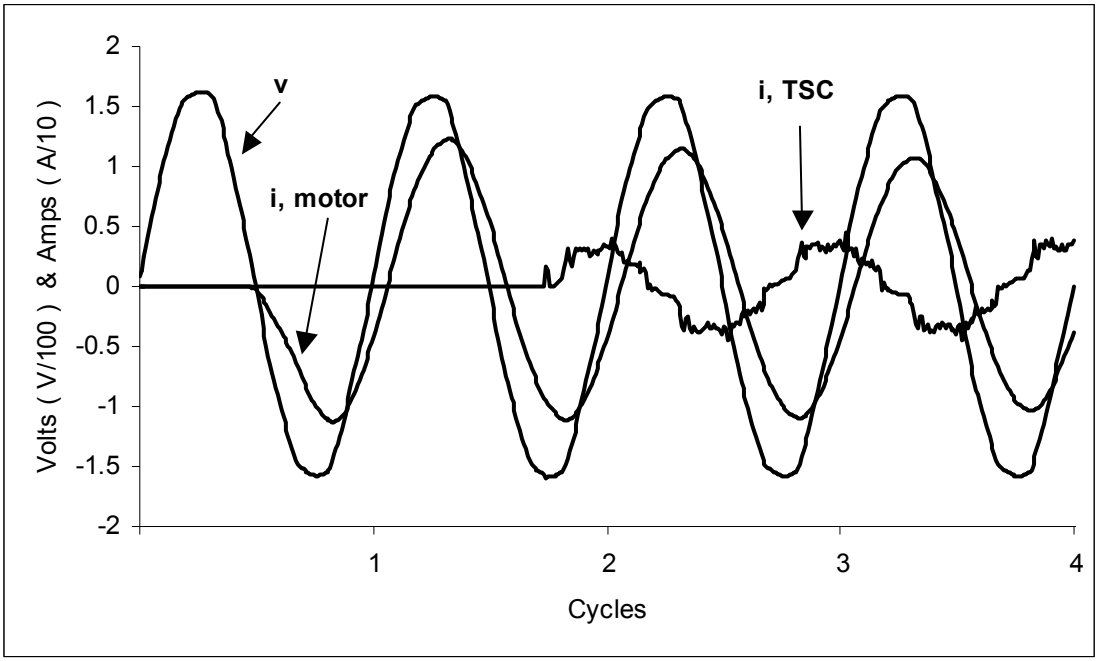

Figure 5.2: Phase-A Voltage, Motor Current, TSC Current During Motor Start

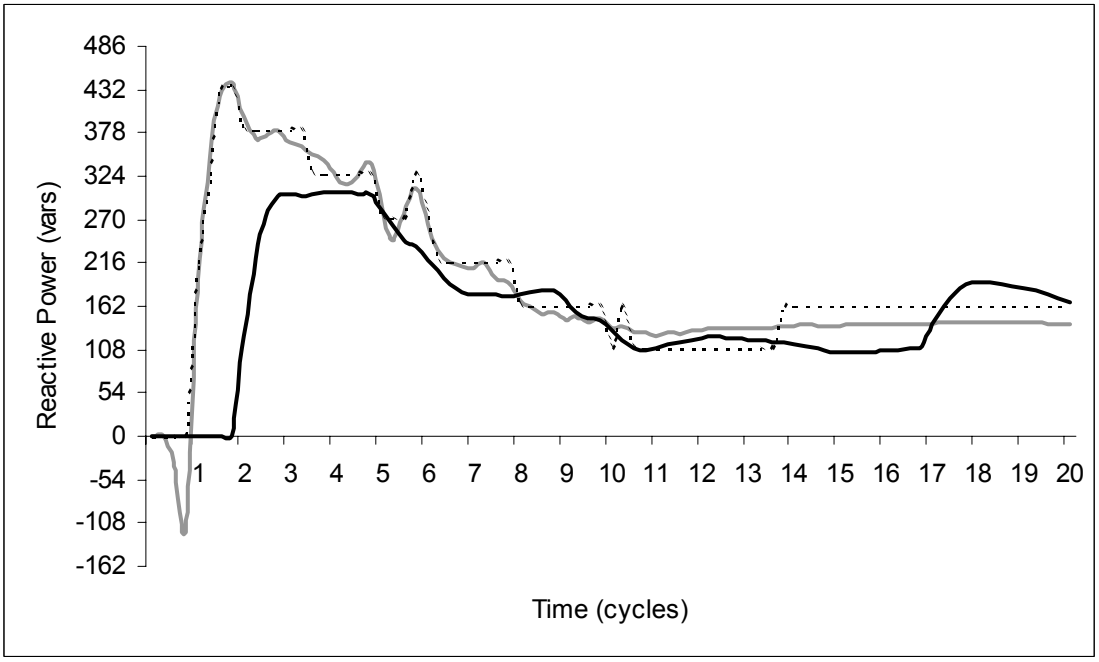

Figure 5.3: Phase-A Reactive Power Demand and Generation

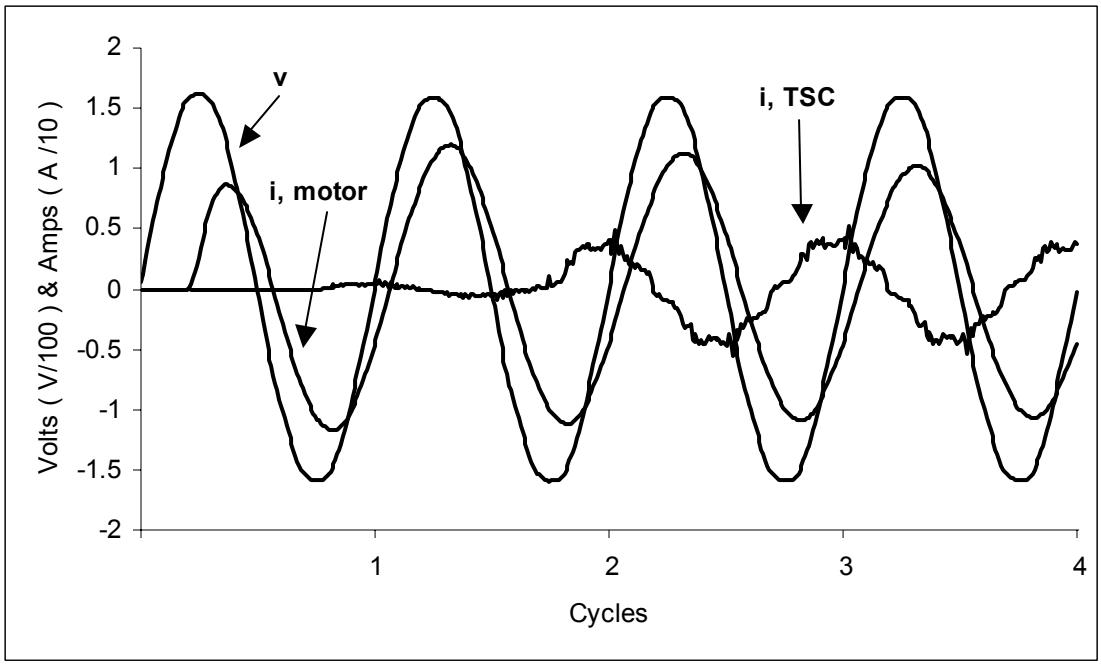

Figure 5.4: Phase-B Voltage, Motor Current, TSC Current During Motor Start

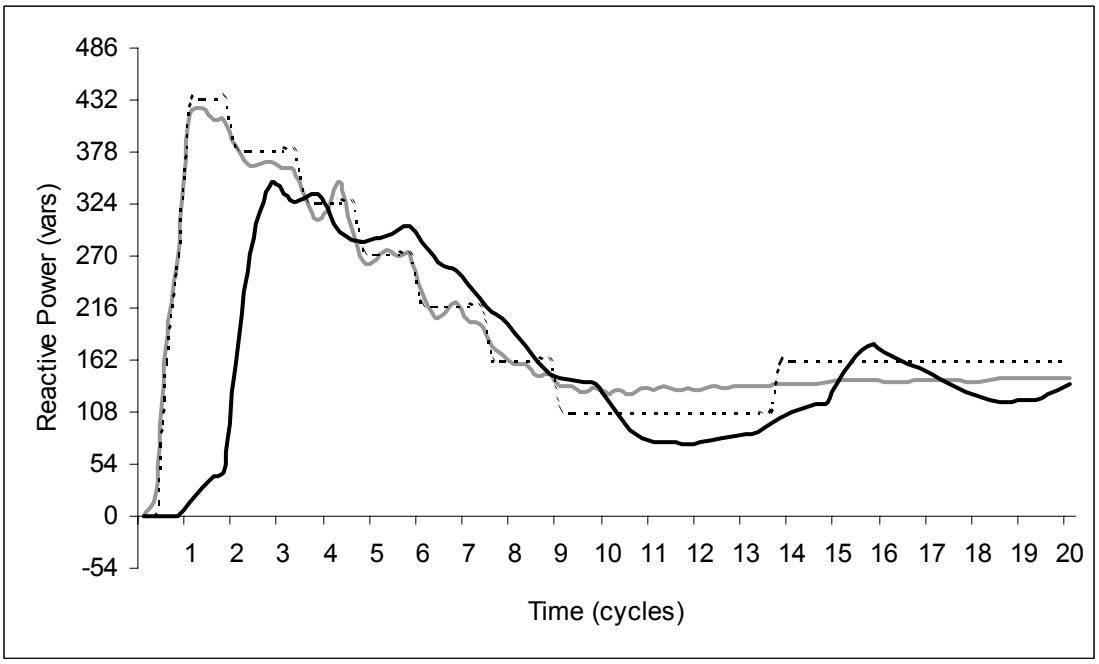

Figure 5.5: Phase-B Reactive Power Demand and Generation

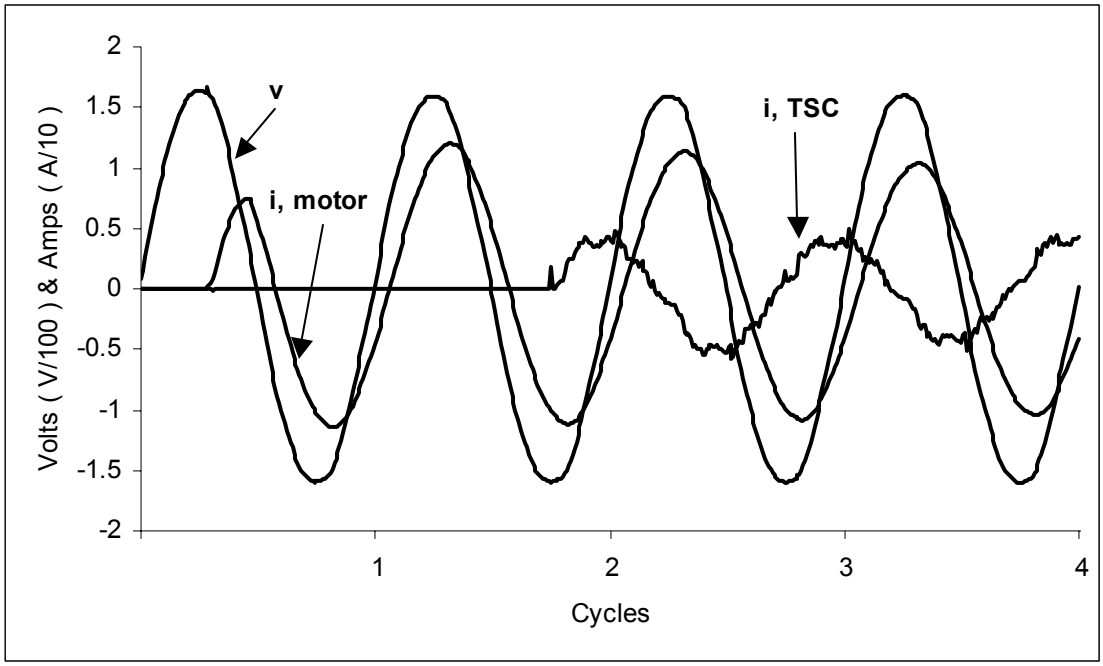

Figure 5.6: Phase-C Voltage, Motor Current, TSC Current During Motor Start

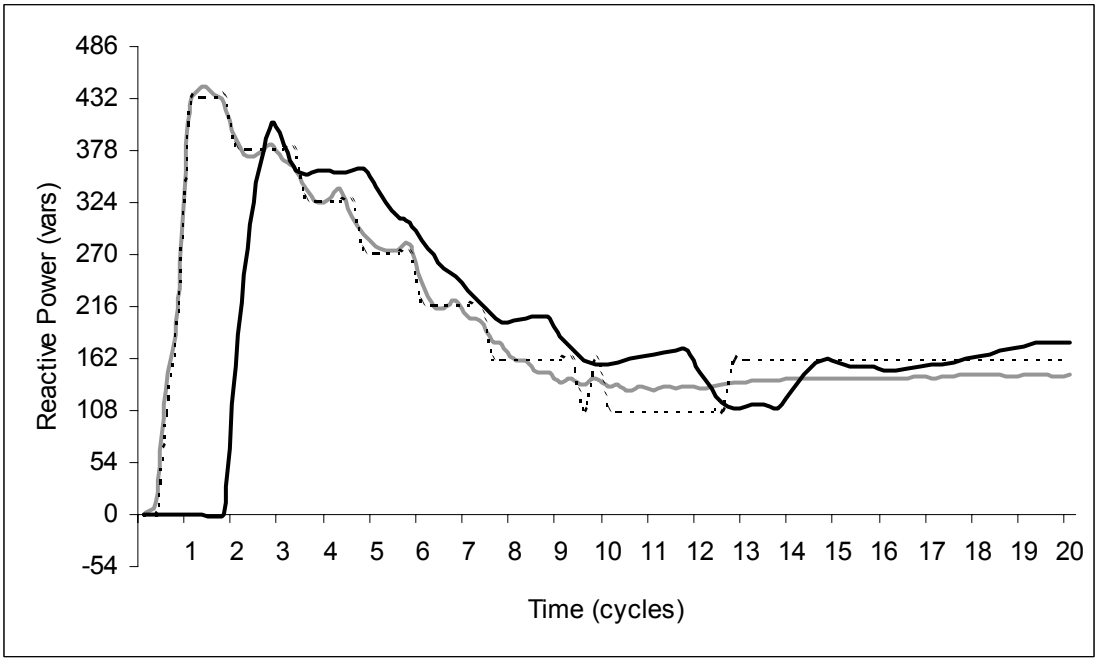

Figure 5.7: Phase-C Reactive Power Demand and Generation

As shown in Figures 5.1 to 5.3, the TSC is able to respond quickly to the reactive demand of the starting induction motor. Again, the reason the reactive generation in the figures does not take the expected step shape is due to the settling time of the filters necessary for the calculation of the reactive power. In actuality, the reactive generation supplied by the TSC is in the step form as the result of the capacitors being fully switched in or out on a per cycle basis.

The initial response delay of the TSC is a result of the limited sampling rate and the application of the switching algorithm coupled with the timing of the gating circuit. Because the application of the switching algorithm is determined by the clock of the PC-104 and is completely independent of any timing of the ac source, situations can arise where the updating of the switching algorithm output after a large change falls after the closest transient free switching point of the capacitors. If this happens, the updated switching algorithm will not reflect the changes in reactive demand. As a result, no reactive generation is switched in until the next transient free switching point is reached.

Even if the value of the reactive demand were updated before the transient free switching point of the capacitors was reached, the settling time of the filters may reduce the effective amount of reactive generation switched in. The maximum settling time of the filters, by design, is one cycle of the signal. If the transient free switching point takes place during this settling time, a lower amount of reactive power demand will be calculated than is actually present. This can be seen by the response of the TSC in phase-B shown in Figure 5.2. When the first transient free switching point arrives a small amount of reactive generation is switched in. At worst case, an accurate response to

large changes will take two cycles, one cycle to accurately measure the reactive demand and another to switch safely.

The discrepancies between the switching logic and the reactive generation after the reactive demand has settled, as shown in Figure 5.3, is a result of the proximity to the half way point between steps in capacitor switching. The reactive demand after start up of the motor settles for a time around 135 var. This reactive demand is right at the 50% mark between the 108 and 162 var steps. Minor variations in applied voltage or motor current will result in a switching change that might be very temporary or that could last indefinitely.

CHAPTER V

CONCLUSION

The purpose of this thesis was to develop and design a fully functional thyristor switched capacitor for potential customer side application. To facilitate the design it was necessary to develop methods to switch the capacitors safely. Instead of thyristors, IGBT modules with a free wheeling diode were selected for the solid-state devices because of their ability to handle medium power levels and their simplicity in gating. Safe switching of the IGBTs and capacitors was obtained by the design of a gating circuit that would limit the switching of the capacitors to transient free points of the waveforms. This gating circuit also served the purpose of protecting the controlling equipment from potentially damaging currents and voltages.

The design also required a quick and accurate response to changing reactive demand. Two methods were evaluated for the calculation of the reactive demand and both were implemented using a microprocessor and data acquisition hardware. The proposed zero crossing method initially seemed to be a viable option, but further simulation showed that it was limited by the unfavorable response to changes in the input signal magnitudes. The least squares method was determined to provide sufficiently accurate reactive power calculations for this application. The least squares method was

implemented on a PC-104 platform so that the controller can be placed in harsh environments.

All of the components were fully realized in a prototype to evaluate the proposed TSC design. Results obtained in actual applications were shown to meet all expectations. While the prototype was not fully packaged for placement in a harsh environment it does provide a strong basis for a mitigation device for customer locations with widely varying reactive power demands.

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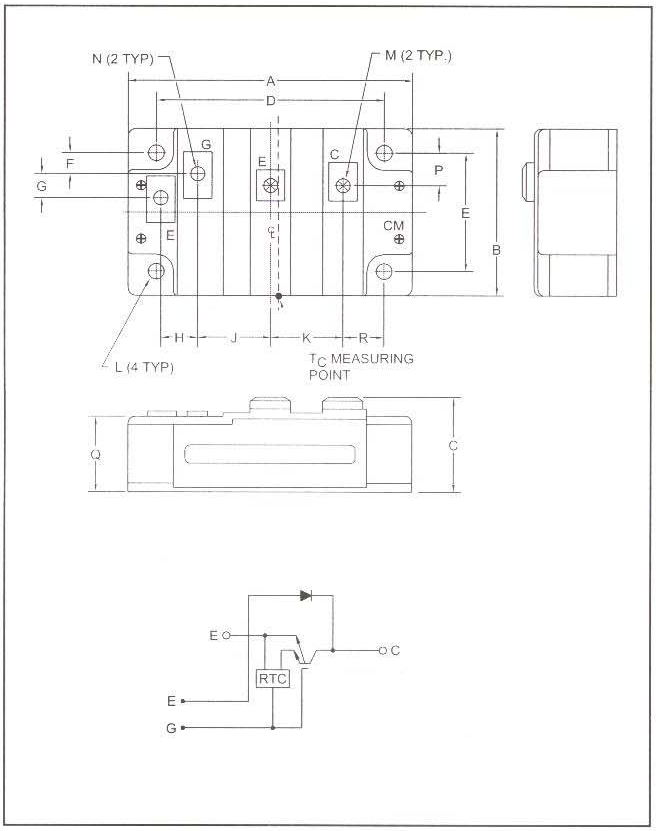
APPENDIX

Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

CM600HU-12F

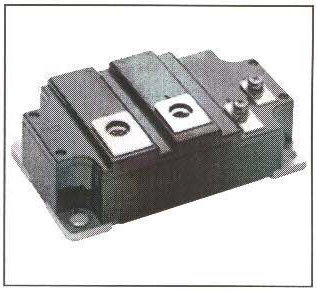
Trench Gate Design Single IGBTMOD™ 600 Amperes/600 Volts



Outline Drawing and Circuit Diagram

Dimensions	Inches	Millimeters
A	4.21	107.0
B	2.44	62.0
C	1.34 +0.04/-0.02	34.0 +1.0/-0.5
D	3.66±0.01	93.0±0.25
E	1.88±0.01	48.0±0.25
F	0.37	9.5
G	0.39	10.0
H	0.53	13.5

Dimensions	Inches	Millimeters
J	1.02	26.0
K	1.14	29.0
L	0.26 Dia	6.5 Dia.
M	M8	M8
N	M4	M4
P	0.49	12.55
Q	1.02 +0.04/-0.02	26.0 +1.0/-0.5
R	0.81	20.5



Description:
Powerex IGBTMOD™ Modules are designed for use in switching applications. Each module consists of one IGBT Transistor in a single configuration with a reverse-connected super-fast recovery free-wheel diode. All components and interconnects are isolated from the heat sinking baseplate, offering simplified system assembly and thermal management.

Features:
- ☐ Low Drive Power
- ☐ Low $V_{CE(sat)}$
- ☐ Discrete Super-Fast Recovery Free-Wheel Diode
- ☐ Isolated Baseplate for Easy Heat Sinking

Applications:
- ☐ AC Motor Control
- ☐ UPS
- ☐ Battery Powered Supplies

Ordering Information:
Example: Select the complete module number you desire from the table - i.e. CM600HU-12F is a 600V (V_{CES}), 600 Ampere Single IGBTMOD™ Power Module.

Type	Current Rating Amperes	V_{CES} Volts (x 50)
CM	600	12

Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

CM600HU-12F
Trench Gate Design Single IGBTMOD™
600 Amperes/600 Volts

Absolute Maximum Ratings, T_j = 25 °C unless otherwise specified

Ratings	Symbol	CM600HU-12F	Units
Junction Temperature	T_j	-40 to 150	°C
Storage Temperature	T_{stg}	-40 to 125	°C
Collector-Emitter Voltage (G-E SHORT)	V_{CES}	600	Volts
Gate-Emitter Voltage (C-E SHORT)	V_{GES}	±20	Volts
Collector Current (T_C = 25°C)	I_C	600	Amperes
Peak Collector Current ($T_j \leq 150°C$)	I_{CM}	1200*	Amperes
Emitter Current** (T_C = 25°C)	I_E	600	Amperes
Peak Emitter Current**	I_{EM}	1200*	Amperes
Maximum Collector Dissipation (T_C = 25°C)	P_C	1420	Watts
Mounting Torque, M8 Main Terminal	–	95	in-lb
Mounting Torque, M6 Mounting	–	40	in-lb
Mounting Torque, M4 Terminal	–	15	in-lb
Weight	–	450	Grams
Isolation Voltage (Main Terminal to Baseplate, AC 1 min.)	V_{iso}	2500	Volts

Static Electrical Characteristics, T_j = 25 °C unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Collector-Cutoff Current	I_{CES}	$V_{CE} = V_{CES}$, V_{GE} = 0V	–	–	1	mA
Gate Leakage Voltage	I_{GES}	$V_{GE} = V_{CES}$, V_{CE} = 0V	–	–	80	µA
Gate-Emitter Threshold Voltage	$V_{GE(th)}$	I_C = 60mA, V_{CE} = 10V	5	6	7	Volts
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 600A, V_{GE} = 15V, T_j = 25°C	–	1.6	2.2	Volts
		I_C = 600A, V_{GE} = 15V, T_j = 125°C	–	1.6	–	Volts
Total Gate Charge	Q_G	V_{CC} = 300V, I_C = 600A, V_{GE} = 15V	–	3720	–	nC
Emitter-Collector Voltage**	V_{EC}	I_E = 600A, V_{GE} = 0V	–	–	2.6	Volts

* Pulse width and repetition rate should be such that the device junction temperature (T_j) does not exceed $T_{j(max)}$ rating.
** Represents characteristics of the anti-parallel, emitter-to-collector free-wheel diode (FWDi).

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CM600HU-12F
Trench Gate Design Single IGBTMOD™
600 Amperes/600 Volts

Dynamic Electrical Characteristics, T_j = 25 °C unless otherwise specified

Characteristics		Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance		C_{ies}		–	–	160	nf
Output Capacitance		C_{oes}	V_{CE} = 10V, V_{GE} = 0V	–	–	11	nf
Reverse Transfer Capacitance		C_{res}		–	–	6	nf
Inductive	Turn-on Delay Time	$t_{d(on)}$	V_{CC} = 300V, I_C = 600A,	–	–	600	ns
Load	Rise Time	t_r	V_{GE1} = V_{GE2} = 15V,	–	–	400	ns
Switch	Turn-off Delay Time	$t_{d(off)}$	R_G = 3.1Ω,	–	–	900	ns
Times	Fall Time	t_f	Inductive Load	–	–	250	ns
Diode Reverse Recovery Time**		t_{rr}	Switching Operation	–	–	300	ns
Diode Reverse Recovery Charge**		Q_{rr}	I_E = 600A	–	11.7	–	µC

Thermal and Mechanical Characteristics, T_j = 25 °C unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Thermal Resistance, Junction to Case	$R_{th(j-c)}Q$	Per IGBT, T_c Reference Point per Outline Drawing	–		0.088	°C/W
Thermal Resistance, Junction to Case	$R_{th(j-c)}D$	Per FWDi, T_c Reference Point per Outline Drawing	–	–	0.12	°C/W
Thermal Resistance, Junction to Case	$R_{th(j-c)'}Q$	Per IGBT, T_c Reference Point Under Chip	–	0.04		°C/W
Contact Thermal Resistance	$R_{th(c-f)}$	Per Module, Thermal Grease Applied	–	0.02	–	°C/W

** Represents characteristics of the anti-parallel, emitter-to-collector free-wheel diode (FWDi).

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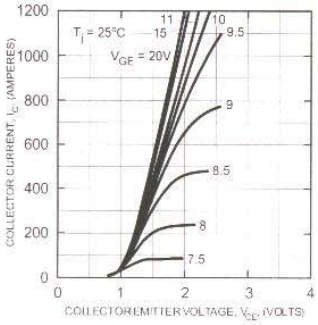
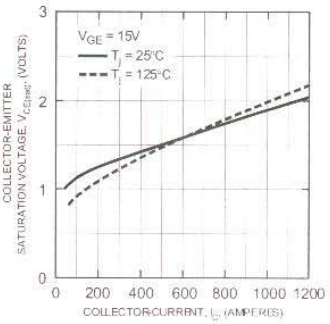
CM600HU-12F
Trench Gate Design Single IGBTMOD™
600 Amperes/600 Volts

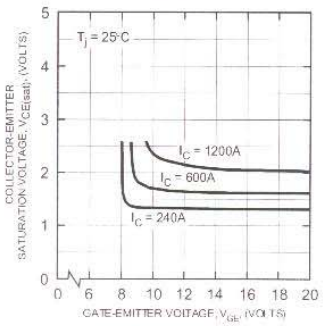
OUTPUT CHARACTERISTICS (TYPICAL)



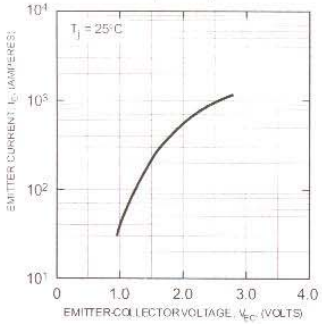
COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)



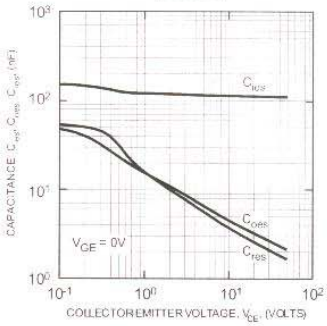
COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)



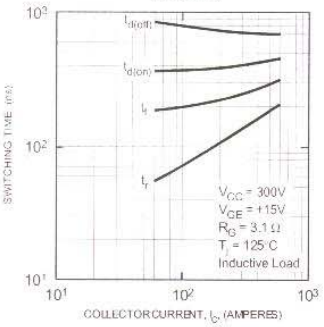
FREE-WHEEL DIODE FORWARD CHARACTERISTICS (TYPICAL)



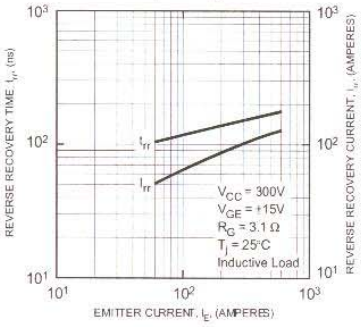
CAPACITANCE VS. V_{CE} (TYPICAL)



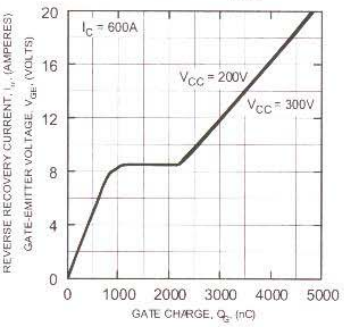
HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)



REVERSE RECOVERY CHARACTERISTICS (TYPICAL)



GATE CHARGE, V_{GE}



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (IGBT & FWDi)